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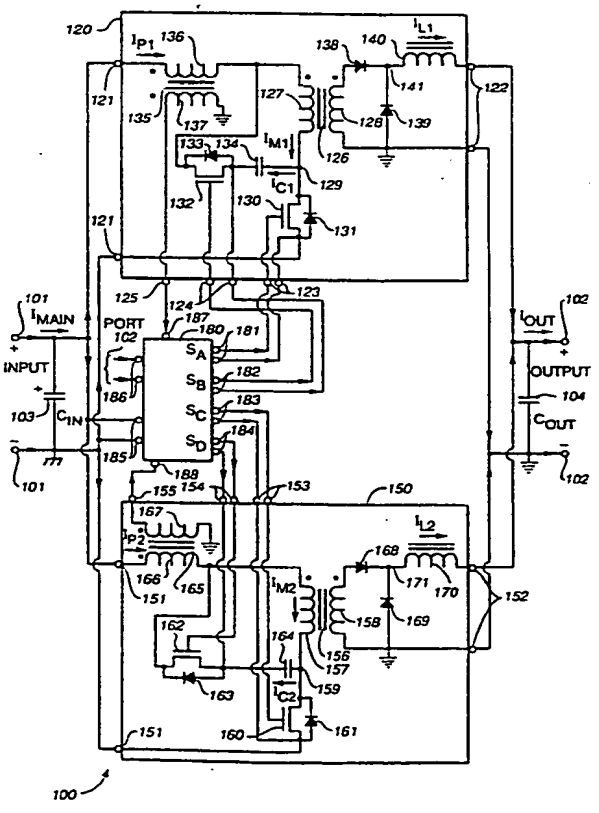
(54) Title: DUAL ACTIVE CLAMP POWER CONVERTER

(57) Abstract

A switching power converter utilizing the single-ended converter topology and active clamp circuitry is described which dramatically reduces the input ripple current seen on the primary input circuit. As a result, a compact, virtually noise-free power converter is provided which further increases conversion efficiency and decreases EMI radiation noise. The power converter comprises two active clamp converters operating at substantially the same switching frequency and at an approximate phase angle difference of 180 degrees. Means are included to combine the input currents of each converter such that the effects of the secondary-circuit ripple currents cancel. As a further feature, means are included to combine the magnetizing currents of each converter such that the fluctuations in the magnetizing currents cancel. Input noise is further reduced by designing the converters to nominally operate at a 50 % duty-cycle at the targeted input voltage level. Owing to its compact size, high efficiency, and small input ripple current characteristics, the present invention is well suited for computer, telephone exchange, and telecommunications applications.



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DUAL ACTIVE CLAMP POWER CONVERTER

FIELD OF THE INVENTION

The present invention relates to switch mode power supplies and, more particularly, to active clamp forward converters configured so as to minimize input and output ripple current.

BACKGROUND OF THE INVENTION

This application relates to the active clamp reset circuit as, for example, described in an article by Bruce Carsten entitled "High Power SMPS Require Intrinsic Reliability", *Proceedings of the Third Annual International PCI '81 Conference*, September 1981, pp 118-133 and in U.S. Patent No. 4,441,146 issued to Vinciarelli. The active clamp reset circuit is applied usually to a single-ended converter, as for example a forward converter or a flyback converter, which comprises a power transformer, a primary switch, an input power source, and a secondary-side distribution circuit. In such a single-ended converter, the primary winding of the converter's power transformer is coupled to the input power source via the primary switch, which periodically switches the primary circuit between 'ON' periods, when energy is extracted from the input power source, and 'OFF' periods.

The active clamp circuit generally comprises a series combination of a 'clamp' capacitor and an 'auxiliary' switch, which is coupled in parallel with one of the power transformer's windings. The auxiliary switch is operated substantially opposite to the primary switch, being closed when the primary switch is open and being open when the primary switch is closed. Thus, during the ON period when the primary switch is closed, the voltage of the input power source is impressed upon the power transformer windings via the primary winding, and during the OFF period when the primary switch is open, the voltage built up on the clamp capacitor is impressed upon the power transformer windings via the winding to which the active clamp circuit is coupled. During steady state operations, the voltage of the clamp capacitor assumes a value which causes the time-integrated voltage on the primary winding to be zero over a cycle of one ON

period followed by a subsequent OFF period (*i.e.*, an equal amount of positive and negative volt-seconds).

The active clamp reset circuit has a number of advantages over the standard forward converter and standard flyback converter in the area of conversion efficiency. One advantage is that the active clamp reset circuit recycles the magnetizing current of the converter's power transformer in such a way that the power transformer's magnetic core may be used to its fullest extent (*i.e.*, both the first and third quadrant of the core's B-H characteristic curve are utilized). Another advantage of the active clamp reset circuit is that the duty cycle on the converter's primary switch can exceed 50% without causing a saturation of the magnetic flux in the power transformer's core. (The duty cycle is the ratio of the ON period to the total switching period T, and is a fraction which ranges between 0.0 and 1.0. For a duty cycle given in percentage, this ratio is multiplied by 100%.) Both of these advantages allow the converter's power transformer to be used more efficiently that the standard forward and flyback converters.

As with the above-mentioned standard converters, however, the active clamp forward converter has the problem of excessive "switching noise" on its input current line. This noise on the input current is due to the ripple effect of the magnetizing current in the primary circuit and the load current in the secondary circuit. The ripple noise has thus far prevented the use of the active clamp converter in low noise applications, such as 48VDC-to-5VDC supplies for telephone exchange equipment. To date, the push-pull converter and the Cuk converter have been extensively used for such low noise applications. However, each of these converters has its respective advantages and disadvantages. The Cuk converter, for example, has the advantage of low input ripple current but has the disadvantage of requiring large transformer coupling capacitors which carry large currents and, therefore, must have a high capacitance value. Presently, high quality polyproylene capacitors and multi-layer ceramic capacitors are typically used for these transformer coupling capacitors. Such capacitors are expensive and generally bulky, adding to both the cost and size of typical implementations of the Cuk converter.

On the other hand, the push-pull converter does not required such large coupling capacitors but it has the disadvantage of a high input ripple current

in comparison to that of the Cuk converter. The minimum input ripple current of a push-pull converter occurs when each of the two primary switches of the push-pull are operated at a duty cycle of 50%, which is the maximum theoretical limit. In practice, the duty cycle must be limited to a lesser value, such as 45%, to ensure that each of the two primary switches do not conduct at the same time, thereby preventing conflicting voltages from being applied at the same time to the power transformer of the push-pull converter. This limiting of the duty cycle raises the input ripple current, since at certain times during the switching cycle no current is being drawn from the input power source. To make matters worse, the minimum input ripple current condition occurs at an extremity of the duty-cycle range, *e.g.*, 45%, and therefore the typical push-pull converter cannot operate with this minimum condition when the input voltage is at its nominal value. This is because the typical push-pull converter is designed to operate at a lower duty-cycle value, for example 25%, when the input voltage is at its nominal value so that the converter can compensate for variations in the input voltage by varying the duty cycle. For example, to compensate for an input voltage value which is less than the nominal value, the converter would increase the duty cycle away from the nominal value.

There is presently a need for a converter whose characteristics match both the lower cost and size of the push-pull converter and the lower input ripple current of the Cuk converter. Additionally, there is presently a need for an inexpensive and compact converter which has its minimum input ripple current occurring near or at the nominal value of the input voltage.

The prior art has attempted to address the input and output ripple current issue by coupling three or more like converters in parallel. The prior art has viewed that at least three converters are necessary for this because the majority of switching converters cannot operate above a 50% duty cycle. Using three converters or more allows the duty cycle to be designed at 0.33 (33%) or less, which gives each converter ample "room" to vary the duty cycle in response to voltage variations in the input and output voltages. For example, in a three converter system the duty-cycle may be centered at 0.33 (33%), and may vary between 0.00 and 0.49 in response to voltage variations. Four parallel coupled converters may therefore be preferred in the prior art, since the duty-cycle may be

nominally set at 0.25 (25%), which is substantially in the center of the allowable range of 0.00 to 0.49. However, the use of three or more converters in this way substantially increases cost and the volumetric size of the total converter.

Presently, there is a great need for a compact, low noise, and highly efficient power converter, which is not being provided by the push-pull and Cuk converter topologies due to their above-described disadvantages and is not being provided by the single-ended forward converter topologies due to their large input ripple current characteristics.

SUMMARY OF THE INVENTION

Consequently, the present invention is directed towards utilizing the compact nature of the single-ended converter topology, specifically the active clamp converter topology, while significantly reducing the input ripple current noise of the single-ended converter topology. The present invention recognizes that the major components of input ripple current in a active clamp forward converter are the secondary-side current, as transformed back to the primary circuit, the magnetizing current, and the current arising from the primary leakage inductance. The present invention also recognizes that the input ripple current of one active clamp forward converter has a characteristic waveform which could be substantially "canceled" by another similar active clamp converter operating at the same switching-frequency but in opposite phase, *i.e.*, at a phase difference of substantially 180 degrees. The present invention further recognizes that two such active clamp converters operated in this manner may replace a single active clamp converter to provide the same output power level, while using substantially the same power transformer core volume and reducing the size of the input filter capacitance. Additionally, the present invention recognizes that two such active clamp converters operated in this manner may provide a lower cost converter for low-noise applications than a Cuk converter operating at comparable power levels.

Broadly stated, the present invention comprises a dual active clamp (DAC) forward converter including two active clamp forward converters connected in parallel and operated in a manner so as to substantially reduce the input ripple current of the DAC converter so that the resultant compact size and low cost of the active clamp forward converters may be exploited for low-noise power supply

applications. More specifically, the present invention comprises an input port for receiving a source of power, an output port for providing power to a load, a first active clamp single-ended converter, and a second active clamp single-ended converter. Each active clamp converter includes a power transformer having a primary winding coupled to the input port and a secondary winding coupled to the output port, a primary switch coupled in series between the primary winding and the input port, and an active clamp circuit including a series combination of an auxiliary switch and a capacitor. In one preferred embodiment of the present invention, the active clamp circuit in each converter is coupled across either the primary winding or the secondary winding of the converter's power transformer.

The present invention further comprises means for generating a first duty-cycle signal and a second duty-cycle signal for controlling the switching state of primary switches in respective converters, each of the first and second duty-cycle signals having a first state and a second state. Each of the first and second duty-cycle signals alternate between its respective first state and its respective second state. Additionally, the second duty-cycle signal is phase-shifted by substantially 180 degrees from the first duty-cycle signal.

The present invention further comprises a first control means responsive to the first duty-cycle signal for operating the primary switch and auxiliary switch of the first converter. The first control means causes the primary switch of the first converter to close substantially when the first duty-cycle signal enters its respective first state, and causes the primary switch of the first converter to open substantially when the first duty-cycle signal enters its respective second state. Additionally, the first control means causes the auxiliary switch of the first converter to open substantially when the first duty-cycle signal enters its respective first state and to close substantially when the first duty-cycle signal enters its respective second state.

The present invention further comprises a second control means responsive to the second duty-cycle signal for operating the primary switch and the auxiliary switch of the second converter. The second control means causes the primary switch of the second converter to close substantially when the second duty-cycle signal enters its respective first state, and causes the primary switch of the second converter to open substantially when the second duty-cycle signal enters

its respective second state. Additionally, the second control means causes the auxiliary switch of the second converter to open substantially when the second duty-cycle signal enters its respective first state and to close substantially when the second duty-cycle signal enters its respective second state. The coupling and operation of the first and second converters in the above described manner significantly reduces the input ripple current and output ripple current at the input and output ports, respectively, of a dual converter according to the present invention.

In another preferred embodiment of the present invention, a means for further reducing the noise effects of the magnetizing current is included. This means comprises the coupling of the series combination of the auxiliary switch and the clamp capacitor of each converter in parallel with the primary switch of its respective converter, instead of coupling the series combination in parallel with one of the power transformer's windings. This particular coupling causes the magnetizing current of each power transformer to flow in a continuous manner in the primary circuit of the corresponding active clamp converter. The magnetizing currents from each of the converters are then coupled in parallel to substantially cancel the ripple components in each of these magnetizing currents.

Accordingly, it is an object of the present invention to provide a low-cost, compact converter having a low input ripple current characteristic.

It is another object of the present invention to minimize the input and output ripple currents of the single-ended converter topology.

It is yet another object of the present invention to recycle the magnetizing current in a manner that increases the overall efficiency of the single-ended power converter topology.

It is yet another object of the present invention to reduce the Electromagnetic Interference (EMI) radiation effects of the single-ended power converter topology.

It is a further object of the present invention to recycle magnetizing current between two active clamp converters to reduce the input ripple current.

These and other objects of the present invention will become apparent to those skilled in the art from the following detailed description of the invention and from the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 is a block diagram of an active clamp forward converter according to the prior art.

FIGURE 2 is a timing diagram of key currents and voltage of the prior art forward converter shown in FIGURE 1.

FIGURE 3 is a first embodiment of the dual active clamp converter according to the present invention.

FIGURE 4 is a second embodiment of the dual active clamp converter according to the present invention.

FIGURE 5 is a timing diagram of key currents and voltages of the dual active clamp forward converter according to the present invention shown in FIGURES 3 and 4.

FIGURE 6 is a second embodiment of the first and second converters according to the present invention.

FIGURE 7 is a more detailed embodiment of the control means according to the present invention.

FIGURE 8 is a timing diagram of key signals of the control means according to the present invention.

FIGURE 9 is a set of graphs comparing the relative input ripple voltage produced by a single active clamp forward converter and by a dual active clamp forward converter according to the present invention.

FIGURE 10 is a schematic diagram of a standard push-pull converter.

FIGURE 11 is a graph comparing the magnitude of input ripple current over a range of input voltages for a prior art push-pull converter and a dual active clamp converter according to the present invention, for comparable amounts of power conversion.

DETAILED DESCRIPTION OF THE INVENTION

The features of the present invention may be better appreciated and comprehended with a more detailed description of active clamp forward converter of the prior art. An exemplary active clamp forward converter according to the prior art is shown FIGURE 1. The prior art converter is coupled between an

input power source V_{IN} and an output load R_L. The input power source typical has a finite amount of input impedance Z_{IN}, which is important to consider at high switching frequencies. The prior art converter also has a power transformer T_1, a primary switch SW_1 for selectively coupling the primary winding of power transformer T_1 to the input power source V_{IN}, a clamp capacitor C_C, and an auxiliary switch SW_2 for selectively coupling clamp capacitor C_C to one of the windings of power transformer T_1 (primary winding as shown in FIGURE 1). For the purposes of simplifying the discussion, power transformer T_1 has a 1:1 turns ratio. Primary switch SW_1 and auxiliary switch SW_2 are operated opposite to one another, SW_2 being open when SW_1 is closed and SW_2 being closed when SW_1 is open. The prior art converter also has a secondary-side circuit comprising rectifiers D_1 and D_2, inductor L_1, and capacitor C_1 for transferring power from the secondary winding of power transformer T_1 to the load R_1, as is well known in the electrical power-converter art.

During operation, clamp capacitor C_C builds up a steady-state voltage across its terminals and, when connected to the primary winding by SW_2, reverses the polarity of applied voltage across the primary winding, as previously applied by the input power source via switch SW_1. As is known in the active clamp converter art, this action serves to "reset" power transformer T_1's core so that it does not magnetically saturate, and also serves to "recycle" the magnetizing energy of power transformer T_1 back to input power source V_{IN}. The series combination of clamp capacitor C_C and auxiliary switch SW_2 are referred to as an "active clamp" in the art because clamp capacitor C_C is used to selective clamp the transformer winding voltage, as determined by the active operation of switch SW_2.

The operation of switches SW_1 and SW_2, along with key voltage and current waveforms of the prior art converter in FIGURE 1, are shown at a timing diagram in FIGURE 2. The graphs labeled as SW_1 and SW_2 show the operation of switches SW_1 and SW_2, respectively, with "ON" and "OFF" labels indicating when each switch is closed and open, respectively. The current provided to the load by the secondary winding is shown in a graph I_S. With reference to FIGURE 1, it can be seen that current is provided to the output load when primary switch SW_1 is closed. As discussed in greater detail below, the secondary current I_S is transformed from the primary circuit and, therefore, shows up as a component of

the current waveforms for the primary winding current and the input source current.

Power transformer T_1 comprises a ferromagnetic core which has a finite amount of magnetic reluctance. As is known in the transformer art, the reluctance gives rise to a "magnetizing current", which flows in one or more of the power transformer's windings at any given time and is required to overcome the magnetic reluctance of the core. A power transformer (*i.e.*, a real transformer) is often modeled as an ideal transformer with an inductor coupled in parallel with one of the windings of the ideal transformer, usually the primary winding, to represent the magnetizing current. The magnetizing current in the prior art converter of FIGURE 1 flows primarily in the primary winding and is shown in the graph labeled as I_M. The magnetizing current increases substantially linearly in time when the voltage from source V_{IN} is applied to the primary winding via switch SW_1 and decreases substantially linearly in time when the reversing voltage from clamp capacitor C_C is applied via switch SW_2. The steady state voltage on capacitor C_C, designated as V_{CC}, is related to the input voltage V_{IN} and the duty-cycle of switch SW_1 such that the magnetizing current is centered around zero amperes during steady-state operations of the active clamp converter. More specifically, given a 1:1 turns ratio for power transformer T_1, the magnitude of the clamp-capacitor voltage is substantially given as follows:

$$V_{CC} = V_{IN}\frac{t_{ON}}{T - t_{ON}} \qquad (1)$$

where t_{ON} is the time duration that switch SW_1 is closed (ON state) and T is the time duration of the switching cycle for switch SW_1. (As is well known in the electrical power converter art, the duty-cycle of switch SW_1 is equal to t_{ON} divided by the switching cycle T.)

Also shown in FIGURE 2 are the waveforms for the current into clamp capacitor C_C, the current into the primary winding of power transformer T_1, and the current from input power source V_{IN}, which is labeled as I_{MAIN}. The current into capacitor C_C is shown at a graph labeled I_{CC} and is substantially equal to the magnetizing current during the ON period of switch SW_2. The current in the primary winding is shown at a graph labeled as I_P and is substantially equal to

the magnetizing current I_M plus the reflected secondary current I_S. Finally, the current waveform for current I_{MAIN} from input power source V_{IN} is shown at a graph labeled as I_{MAIN} and is, by Kirchhoff's current law, equal to the primary winding current I_P waveform less the clamp-capacitor current I_{CC} waveform.

As can be seen by FIGURE 2, both the input current I_{MAIN} and the secondary current I_S are pulsed in nature and, consequently, are considered to be relatively noisy, particularly in comparison with the corresponding waveforms for a push-pull converter. Due to the finite input impedance Z_{IN} of the input power source, the noise in the input current I_{MAIN} translates into ripple voltage at the input, which may be coupled to other components and systems being powered by power source V_{IN}. Such coupling may cause a performance degradation or unwanted effects in these other components and systems. In addition, the pulsed nature of the input and output currents may also increase Electro-Magnetic Interference (EMI) effects, particularly at high switching frequencies of 1MHz to 2MHz. This is because the power supply lines to the converter input and the lines to output load can be quite long and can, therefore, act as radiating antennae.

The above problems in the prior art are addressed by the combination of two active clamp forward converters according to the present invention. A first embodiment of the dual active clamp forward converter according to the present invention is shown at 100 in Figure 3. Dual active clamp (DAC) converter 100 includes an input port 101 for receiving a source of input power to be converted and an output port 102 for providing converted power derived from input port 101. Additionally, DAC converter 100 comprises an input capacitor 103 coupled across input port 101 and an output capacitor 104 coupled across output port 102. DAC converter 100 further comprises a first active clamp converter 120, a second active clamp converter 150, and a control means 180 for coordinating the operation of converters 120 and 150. First and second converters 120 and 150 preferably comprise forward-converter topologies. First converter 120, second converter 150, and control means 180 are each described below in greater detail.

First converter 120 includes an input port 121 coupled to input port 101 for receiving the source of input power, and output port 122 coupled to output port 102 for providing power to an output load, and control ports 123 and 124 for

receiving control signals from control means 180 for controlling the switches of converter 120, each of which is described below in greater detail. Additionally, first converter 120 comprises a power transformer 126 having a primary winding 127 coupled to input port 121 and a secondary winding 128 for coupling power to output port 122. First converter 120 further comprises a current sense transformer 135 for sensing the current flowing into the primary circuit of first converter 120. Sense transformer 135 includes a primary winding 136 having a first terminal coupled to the positive terminal of port 121 and a second terminal coupled to primary winding 127 of power transformer 126. Sense transformer 135 further includes a secondary winding 137 having a first terminal coupled to ground and a second terminal coupled to a current sense output port 125 of first converter 120.

Sense transformer 135 provides a current at port 125 which is proportional to that of the current being drawn from the input supply at port 101 by converter 120. As described below in greater detail, the current signal at port 125 is used by control means 180 in controlling the duration switches 130 and 132 are closed. In a preferred embodiment of the present invention, sense transformer 135 has a turns ratio of 1:40 (primary:secondary) and the current provided to port 125 is substantially 1/40th of the current being drawn by the primary circuit of converter 120. As such, very little voltage is dropped across sense transformer 135, typically less than 25mV. Thus, for the purpose of describing the operation of first converter 120, it will be assumed that the voltage drop across current sense transformer 135 does not affect the operation of first converter 120.

First converter 120 further comprises a primary switch 130, a clamp capacitor 134, and an auxiliary switch 132. In the preferred embodiment of the present invention, each of switches 130 and 132 comprises a transistor device having a control terminal (gate) and two conduction terminals (source and drain). The gate and source terminals of primary switch 130 are coupled to control port 123 and the gate and source terminals of auxiliary switch 132 are coupled to control port 124. Each of ports 123 and 124 includes two terminals for receiving two signal lines for respective coupling to these gate and source terminals. In a preferred embodiment of the present invention, each of transistor switches 130 and 132 comprises a MOSFET field effect device, preferably with a corresponding integral body diode 131 and 133, respectively. However, it may be appreciated

that each of switches 130 and 132 may alternatively comprise other transistor devices, such as bipolar-junction transistors (BJTs).

Regarding the arrangement of these components, primary switch 130 is coupled in series with primary winding 127 at a node 129, with the series combination of primary switch 130 and primary winding 127 being coupled to input port 121 by way of sense transformer 135. Additionally, clamp capacitor 134 and auxiliary switch 132 are coupled in series, and this series combination is coupled between node 129 and primary winding 136 of sense transformer 135. In the embodiment of the present invention shown in FIGURE 3, this series combination is coupled such that it is in parallel with primary winding 127. However, as discussed below with reference to another embodiment of the present invention, the series combination of auxiliary switch 132 and clamp capacitor 134 may also be coupled such that it is in parallel with primary switch 130.

In the operation of first converter 120, primary switch 130 is first rendered conductive during an ON period by control means 180 and then rendered non-conductive during a subsequent OFF period by control means 180. The ON period followed by the subsequent OFF period comprises a switching cycle for primary switch 130 and, in turn, a switching cycle for first converter 100. In the preferred operation, first converter 120 is continuous switched with successive switching cycles by control means 180.

For the secondary-side circuit, first converter 120 further comprises rectifiers 138 and 139, and a filter inductor 140. Rectifier 138 and inductor 140 are coupled in series at an intermediate node 141, and this series combination is coupled in series between the first terminal of secondary winding 128 and one terminal of output port 122. The other terminal of output port 122 is coupled to the second terminal of secondary winding 128. Rectifier 139, which functions as a "free-wheeling diode" for inductor 140, is coupled between the second terminal of secondary winding 128 and node 141. In general, rectifiers 138 and 139 form a commutating relationship in which one of rectifiers 139 and 139 blocks current while the other conducts current. Rectifier 138 serves to direct current from secondary winding 128 to a load coupled to output port 102 during predetermined portions of first converter 120's switching cycle (*e.g.*, during the ON period). This conduction of current by rectifier 138 builds up a current in filter inductor

140. When rectifier 138 is not conducting current, rectifier 139 serves to complete a conduction path for the current initiated in filter inductor 140. In FIGURE 3, the current through inductor 140, which is also the current delivered to the load via output port 102, is designated as current I_{L1}.

In the operation of first converter 120, a substantially DC voltage is applied to input port 121 and appropriate control signals from control means 180 are applied to control ports 123 and 124 to operate switches 130 and 132, respectively. As described above, the switching cycle of first converter 120 comprises an ON period in which primary switch 130 is conducting and a subsequent OFF period in which primary switch 130 is not conducting. Auxiliary switch 132 operates essentially opposite to this such that it conducts during a substantial portion of the OFF period and is not conducting during the ON period. Furthermore, primary switch 130 and auxiliary switch 132 preferably operate in a non-overlapping manner where neither switch is conducting at the same time. Preferably, each of switches 130 and 132 is not conducting during the first portion of the OFF period and during the last portion of the OFF period.

During the ON period of first converter 120, primary switch 130 is conducting and the input voltage at input port 121 is applied across primary winding 127. As a result of transformer action, a secondary voltage and current are directed towards output port 122 from secondary winding 128. The current from secondary winding 128 is a function of the voltage across the secondary winding, the voltage at output port 102, the inductance of inductor 140, and the current I_{L1} flowing in inductor 140 at the beginning of the ON period, as is known in the active clamp forward converter art. The current in secondary winding 128 is reflected to primary winding 127, the reflected amount being a function of the turns ratio of power transformer 126. For the purposes of discussing specific numerical quantities associated with converter 120, and without loss of generality, the turns ratio for power transformer 126 is taken to be 4:1 (primary:secondary).

Also during the ON period, a magnetizing current I_{M1} due to the magnetizing inductance of power transformer 126 is conducted through primary winding 127 along with the reflected secondary current. The magnetizing current increases linearly with time and at a substantially constant rate during the ON period. In other words, the magnetizing current I_{M1} is a function of time

substantially governed by the equation $V_P=L_{M1}*(dI_{M1}/dt)$, where L_{M1} is a constant representing the value of the magnetizing inductance and V_P is the voltage across the primary winding. During the ON period, the rate of increase in the magnetizing current I_{M1} is proportional to the applied voltage from input port 121. As is known to the active clamp converter art, the magnetizing current I_{M1} preferable starts at a negative value at the beginning of the ON period and ends at a positive value at the end of the ON period. As discussed below in greater detail, a negative voltage is applied to primary winding 127 during the OFF period which causes the magnetizing current I_{M1} to decrease to a negative value by the end of the OFF period and, consequently, by the start of the ON period.

At the end of the ON period switch 130 is rendered nonconductive by the control signal at port 123. The magnetizing current that has been built up during the ON period continues to flow and flows into the parasitic capacitance associated with node 129. A short time into the OFF period, auxiliary switch 132 is rendered conductive by the control signal at port 124. This couples clamp capacitor 134 across primary winding 127. As a result, the magnetizing current flowing from primary winding 127 is directed into clamp capacitor 134. In FIGURE 3, the reference direction for this current flow into clamp capacitor is given by the current designation I_{C1}. Clamp capacitor 134 applies a reverse (negative) voltage across primary 127 to reduce the magnetizing current, and, ultimately reverse it by the end of the OFF period. Also because of the negative voltage, a negative voltage is applied across secondary winding 128 and rectifier 138 becomes reversed biased. As a result, power is not coupled from power transformer 126 to output port 122 during the OFF period. In its place, "free-wheeling" rectifier 139 allows inductor 140 to continue providing current and power to output port 102.

The total current flow into first converter 120 is shown by the current designation I_{P1} at input port 121. Current I_{P1} represents the current flow into first converter 120 and is equal to the sum of the magnetizing current I_{M1} and the reflected current of secondary winding 128 (*e.g.*, the reflected I_{L1} during ON periods) less the current I_{C1} through clamp capacitor 134. In mathematical terms, this is stated as $I_{P1}=I_{M1}+I_{SR1}-I_{C1}$, where the notation I_{SR1} represent the current in secondary winding 128 which is reflected to primary winding 127. The

subtraction of, rather than the addition of, the clamp capacitor current I_{C1} in this embodiment of the present invention is due to the choice of the reference direction into capacitor 134 from node 129.

As discussed above, the magnetizing current I_{M1} is first directed into clamp capacitor 134 during the first half of the OFF period and then reversed and directed out of clamp capacitor 134 towards node 129 during the second half of the OFF period. Because the current path into clamp capacitor 134 is completed via a path which is in parallel with primary winding 127, the magnetizing current I_{M1} and clamp-capacitor current I_{C1} cancel one another in the relationship for I_{P1} during the OFF period. Thus, the reversal of the magnetizing current I_M during the OFF period is not coupled to the input source connected to input port 121.

Related to the above-described operation of converter 120, the flow of magnetizing current I_{M1} into the parasitic capacitance associated with node 129 before auxiliary switch 132 becomes conductive may raise the voltage of node 129 to a value which renders integrated body diode 133 conductive. This allows clamp capacitor 134 to apply the negative voltage to primary winding 127 before auxiliary switch 132 is rendered conductive by the control signal at port 124. This action does not cause any detrimental effects for converter 120 and may be beneficial in that it may allow the "timing" of the control signal at control port 124 to be "relaxed".

In practice, there is a relationship between the positive voltage applied to primary winding 127 during the ON period and the negative voltage applied during the OFF period. More specifically, the integral of negative voltage applied to primary winding 127 during the OFF period (*i.e.*, the total number of negative volt-seconds) plus the integral of the positive voltage applied to primary winding 127 during the ON period (*i.e.*, the total number of positive volt-seconds) is substantially equal to zero for each switching cycle, during steady-state operation. This ensures that the core of power transformer 126 does not saturate. As is known in the active clamp converter art, the voltage on clamp capacitor 134 obtains a value during steady operations which allows the total integrated volt seconds applied to primary 127 over a switching cycle to be zero.

At the end of the OFF period, the control signal at port 124 directs auxiliary switch 132 to become non-conductive. The magnetizing current I_{M1}

continues to flow in primary winding 127 in a direction towards input port 121 (*i.e.*, a negative value). With auxiliary switch 132 off, the conduction current path for I_{M1} occurs through the parasitic capacitance associated with node 129. As a result, I_{M1} discharges the voltage at node 129. A short time later, the control signal at port 123 instructs primary switch to become conductive, thus beginning the next ON period. In this regard, the negative current flow of I_{M1} may cause integral body diode 131 of primary switch 130 to conduct before the control signal at port 123 instructs primary switch 130 to conduct. This action does not cause any detrimental effects for converter 120 and may be beneficial as it may allow the "timing" of the control signal at control port 123 to be "relaxed".

With regard to the secondary circuit in operation, diode 138 conducts forward current during on the ON period towards output port 122 and blocks current during the OFF period. The current from rectifier 138 is directed towards inductor 140 (diode 138 is not conducting), which builds up a DC component flowing through inductor 140 during steady state operations. During the OFF period, rectifier 139, the so called "free-wheeling diode", conducts the current I_{L1} of inductor 140. Table I lists the component values for a preferred embodiment of DAC converter 100 which provides a 44VDC-to-5VDC converter capable of providing a maximum output current of 40A.

Input Capacitor 103	1.8uF, 100V
Output Capacitor 104	96uF, 10V (Two 47uF Capacitors)
Power Transformer 126	Turns ratio = 8:2 = 4:1 (pri:sec)
Transistor 130	IRFP250 (International Rectifier)
Transistor 132	IRFR220 (International Rectifier)
Capacitor 134	47nF, 200V
Sense Transformer 135	Turns ratio = 1:40 (pri:sec)
Rectifiers 138, 139	0.5V forward Voltage
Inductor 140	1.8uH
Switching Frequency	500KHz

TABLE I.

A description of the structure and operation of first converter 120 has thus far been given. A similar description is now given for second converter

150. In a preferred embodiment of the present invention, second converter 150 is substantially identical in structure and operation to converter 120, with one exception being that the switching cycle for converter 150 is substantially different. This difference is discussed below in greater detail with reference to the operation of control means 180.

Second converter 150 includes an input port 151 coupled to input port 101 for receiving the source of input power, an output port 152 coupled to output port 102 for providing power to an output load, two control ports 153 and 154 for receiving control signals from control means 180 for controlling the switches of converter 150 and a current sense output port 155. Each of ports 153-155 are described below in greater detail. Additionally, second converter 150 comprises a power transformer 156 having a primary winding 157 coupled to input port 151 and a secondary winding 158 for coupling power to output port 152. Second converter 150 further comprises a current sense transformer 165 for sensing the current flowing into the primary circuit of second converter 150. Sense transformer 165 includes a primary winding 166 having a first terminal coupled to the positive terminal of port 151 and a second terminal coupled to primary winding 157 of power transformer 156. Sense transformer 165 further includes a secondary winding 167 having a first terminal coupled to ground and a second terminal coupled to current sense output port 155.

Second converter 150 further comprises a primary switch 160, a clamp capacitor 164, and an auxiliary switch 162. In the preferred embodiment of the present invention, each of switches 160 and 162 comprises a transistor device having a control terminal (gate) and two conduction terminals (source and drain). The gate and source terminals of primary switch 160 are coupled to control port 153 and the gate and source terminals of transistor 162 are coupled to control port 154. Each of ports 153 and 154 includes two terminals for receiving two signal lines for respective coupling to these gate and source terminals. Also in a preferred embodiment of the present invention, each of transistor switches 160 and 162 comprises a MOSFET field effect device, preferably with a corresponding integral body diode 161 and 163, respectively. However, it may be appreciated that each of switches 160 and 162 may alternatively comprise other transistor devices, such as bipolar-junction transistors (BJTs).

Second converter 150 further comprises a node 159, a secondary-side rectifier 168, a free-wheeling rectifier 169, a filter inductor 170, and a second node 171. The components 156, 157, 158, 159, 160, 161, 162, 163, 164, 165, 166, 167, 168, 169, 170, and 171 of second converter 150 correspond in function to the components 126, 127, 128, 129, 130, 131, 132, 133, 134, 135, 136, 137, 138, 139, 140, and 141; respectively, of first converter 120. Additionally, the arrangement of these components of second converter 150 is the same as the arrangement of the components of first converter 120. Furthermore, the basic operation of second converter 150 is the same as that for first converter 120 and the above description of operation for converter 120 is herein applied to describe the operation of second converter 150. As with converter 120, second converter 150 has a magnetizing current I_{M2} flowing in power transformer 156, a primary input current I_{P2} flowing in from port 121, a current I_{C2} flowing into clamp capacitor 164, and an output inductor current I_{L2} flowing through output filter inductor 170. Reference designations for each of these current is shown in FIGURE 3.

Having thus described the structure and operation of first converter 120 and second converter 150, the operation of control means 180 and the coordination of operating converters 120 and 150 are now described. For first converter 120, control means 180 includes an output control port 181 coupled to input control port 123 for providing a control signal to primary switch 130 and an output control port 182 coupled to input control port 124 for providing a control signal to auxiliary switch 132. Each of ports 181 and 182 comprises two terminals which are coupled to respective terminals of input ports 123 and 124, respective. In a preferred embodiment of DAC converter 100, each of the control signals at ports 181 and 182 appears as a voltage across the terminals of ports 181 and 182, respectively. For second converter 150, control means 180 further includes an output control port 183 coupled to input control port 153 for providing a control signal to primary switch 150 and an output control port 184 coupled to input control port 154 for providing a control signal to auxiliary switch 162. Each of ports 183 and 184 comprises two terminals which are coupled to respective terminals of input ports 153 and 154, respectively. In a preferred embodiment of

DAC converter 100, each of the control signals at ports 183 and 184 appears as a voltage across the terminals of ports 183 and 184, respectively.

Control means 180 further includes a power port 185 coupled to input port 101 for receiving a source of power and an output monitoring port 186 coupled to output 102 for receiving the voltage provided to port 102. Control means 180 further includes an input port 187 coupled to port 125 of first converter 120 for receiving a signal representative of the primary current of converter 120 and an input port 188 coupled to port 155 of second converter 150 for receiving a signal representative of the primary current of converter 150. As described below in greater detail, control means 180 senses the output voltage at port 102 via port 186 and respective converter primary currents at ports 187 and 188, and, in response thereto, adjusts the duty-cycle of the control signals present on control ports 181-184.

In operation, control means 180 coordinates the operation of first converter 120 and second converter 150 such that the amount of ripple current at input port 101 is minimized. This is done by providing coordinated pulse-width modulated signals to ports 181-184, the signals having a common switching cycle period T, or time duration T, which is preferably substantially constant during operation of DAC converter 100. These signals, along with key currents of converters 120 and 150, are shown as a function of time by a timing diagram at 300 in FIGURE 5. Specifically, the signals at ports 181-184 are shown by graphs 301-304, respectively.

In a preferred embodiment of DAC converter 100, each of the signals at ports 181-184 has a "resting" state of substantially zero volts and a "pulse" state of substantially 10 volts, as seen in graphs 301-304. For each of ports 181-184, the voltage appears across the port's terminals, and in turn, across the gate and source terminals of the MOSFET transistor coupled to the port. In the pulse state, a positive voltage is applied between the gate and source terminals, with the gate terminal being more positive. The signals at ports 181 and 182 are complimentary to one another and the signals at ports 183 and 184 are complimentary to one another. For example, the signal at port 181 is in its pulse state when the signal at port 182 is in its resting state, and the signal at port 182 is in its pulse state when the signal at port 181 is in its resting state. The ensures

that switches 130 and 132 are switched opposite to one another and that neither are conducting at the same time. The same applies to switches 160 and 162 of second converter 150.

Each of the control signals at ports 181 and 183 starts its respective switching cycle with its pulse state, thereby being in its pulse state during the beginning portion of its switching period T and being in its resting state during the latter portion of its switching period T (time duration T). Additionally, the control signal at port 183, which is for primary switch 160 of second converter 150, starts its switching cycle substantially one-half switching-cycle period (T/2) after the control signal at port 181 starts its switching cycle, the signal at port 181 being for the primary switch of first converter 120. Thus, converters 120 and 150 operate substantially 180 degrees out of phase. This offset is shown in graph 303.

Also in a preferred embodiment of the present invention, the duty cycle of the control signals at ports 181 and 183 is nominally set to a value of substantially 0.50 (50%). The duty cycle is the ratio of the ON period to the switching period T, and is a fraction which ranges between 0.0 and 1.0. (For a duty cycle given in percentage, this ratio is multiplied by 100%: (ON-period)/T*100%.) Additionally, the control signals at ports 181 and 183 are coordinated to have substantially the same duty cycle during operation. The pulse duration of the control signals at ports 181 and 183 for the primary switches is equal to the duty cycle times the period T: (duty cycle)*T. The pulse duration of the control signals at ports 182 and 184 for the auxiliary switches is equal to the fraction 1.0 less the duty cycle, the difference multiplied by the period T: (1 - (duty cycle))*T.

In a further embodiment of the present invention, the duty cycle for the control signals at ports 181 and 183 (for the primary switches) is targeted for a nominal operating value of substantially 0.50 (50%) and an operating range of 0.30 (30%) to 0.70 (70%). This allows a substantial amount of ripple-current reduction during nominal operation at 0.50 (50%) and allows for compensating over- and under-voltages at the input by moving the duty-cycle towards 0.30 (30%) and 0.70 (70%), respectively, while still maintaining good input and output ripple current characteristics. Examples of the input and output ripple reduction as a function of duty-cycle are provided below.

In a preferred embodiment of the present invention, the duty cycle for the control signals at ports 181 and 183 (for the primary switches) ranges between 0.40 and 0.65 about a nominal value of 0.50. As such, the corresponding, complimentary duty cycle for the control signals at ports 182 and 184 (for the auxiliary switches) ranges between 0.60 and 0.35. As is known in the forward converter art, the duty cycle for the primary switches (ports 181 and 183) is adjusted to regulate the voltage at output port 102 and to compensate for variations in the voltage at input port 101. If the output voltage decreases from its targeted nominal value, control means 180 increases the duty cycle to provide more current to output capacitor 104 and the load at port 102 in order to increase the output voltage. If the output voltage increases above its nominal value, the duty cycle is decreased to provide less current. If the input voltage decreases from its nominal value, less voltage is provided to the secondary circuits of converters 120 and 150 during their respective ON periods and, hence, less energy is coupled to the output by the secondary circuits. To compensate for the energy loss, control means 180 increases the duration of the ON periods to increase the amount of energy coupled so as to maintain the output voltage at its nominal value.

The steady state output voltage for each of converters 120 and 150 under nominal current loads is related to the input voltage and duty-cycle by the following equation:

$$(V_{OUT}+V_F) = \frac{(DutyCycle)*V_{IN}}{N_{TURNS}} \qquad (2)$$

where V_{OUT} is the output voltage, V_F is the voltage losses in the secondary circuit (mainly from the commutating rectifiers, such as rectifiers 138 and 139), V_{IN} is the input voltage, and N_{TURNS} is the turns ratio of the power transformer, such as 126 and 156 (number of primary turns divided by the number of secondary turns). In the present invention, the duty cycle is varied in response to changes in the input voltage, so as to maintain the output voltage V_{OUT} at a targeted nominal value.

To realized a 50% duty cycle operation for converters 120 and 150 at the nominal output voltage $V_{OUT,NOM}$, the ratio of the nominal input voltage $V_{IN,NOM}$ to the transformer turns ratio N_{TURNS} is set as follows:

$$\frac{V_{IN.NOM}}{N_{TURNS}} = \frac{(V_{OUT.NOM} + V_F)}{0.50} \qquad (3)$$

Generally, the nominal input voltage $V_{IN,NOM}$ is a given parameter, *i.e.*, a constraint, leaving the transformer turns ratio N_{TURNS} as the parameter to be chosen to satisfy equation (3). For example, if DAC converter 100 is to have a nominal input voltage of $V_{IN,NOM}$=48V with a nominal output voltage of $V_{OUT,NOM}$=5V and a typical voltage loss V_F of 0.5V, the transformer turns ratio N_{TURNS} for each converter 120 and 150 would be substantially set to 4.36:1, or 13:3, to satisfy equation (3). In this way, the transformer turns ratio may be used to effectively set the duty cycle for each of converters 120 and 150 to substantially 50% (0.50) for operation at the given nominal input voltage and nominal output voltage. For a nominal input voltage of 44V and a nominal output voltage of 5V, N_{TURNS} would be substantially 4:1, or an integer multiple thereof. As described below in greater detail, control means 180 operates to keep the output voltage close to the nominal output voltage. Thus, when the input voltage is at its nominal value, control means 180 operates to keep the duty cycle for each of converters 120 and 150 near 50%.

For generating the control signals at port 181-184, control means 180 further comprises a pulse width modulation (PWM) means for generating a first duty-cycle signal for controlling first converter 120 and a second duty-cycle signal for controlling second converter 150. Each of the first and second duty-cycle signals has a first state and a second state, and each alternates in time between its respective first and second states. Additionally, the second duty-cycle signal is phase-shifted in time by substantially 180 degrees from the first duty-cycle signal. In a preferred embodiment of the present invention and as described below in greater detail, the first duty-cycle signal is coupled to port 181 (for primary switch 130 of converter 120) substantially unchanged and the second duty-cycle signal is coupled to port 183 (for primary switch 160 of converter 150) substantially unchanged. Each of the duty-cycle signals is generated as a function

of the measured output voltage and the targeted nominal output voltage such that the output voltage is regulated to be within a specified range around the nominal output voltage. An exemplary range is ±10mV around a nominal output voltage of 5V. In a preferred embodiment of DAC converter 100, each of the duty-cycle signals is also a function of the primary input current of its respective converter (current-mode control). In turn, the primary input current waveform is a function of the input voltage, as described in greater detail below, thereby making each of the duty cycle signals a function of the input voltage. As such, with the transformer turns ratio N_{TURNS} for each converter 120 and 150 set for 50% duty-cycle operation as described above, each of the duty cycle signals is substantially 0.50 (50%) when the input and output voltages are at their respective nominal values.

As indicated above, the auxiliary switches 132 and 162 are operated in a complimentary manner with respect to their corresponding primary switches 130 and 160, respectively. For this, control means 180 further comprises a first control means responsive to the first duty-cycle signal for operating primary switch 130 and auxiliary switch 132 of first converter 120 in a complimentary manner. Specifically, the first control means generates a signal at port 181 to cause primary switch 130 to close substantially when the first duty-cycle signal enters its respective first state, and to cause primary switch 130 to open substantially when the first duty-cycle signal enters its respective second state. Additionally, the first control means generates a signal at port 182 to cause auxiliary switch 132 to open substantially when the first duty-cycle signal enters its respective first state, and to close substantially when the first duty-cycle signal enters its respective second state. In a preferred embodiment of the present invention, the signals at ports 181 and 182 are non-overlapping such that switches 130 and 132 are not rendered conductive at the same time.

In a similar manner, control means 180 further comprises a second control means responsive to the second duty-cycle signal for operating primary switch 160 and auxiliary switch 162 of second converter 150 in a complimentary manner. Specifically, the second control means generates a signal at port 183 to cause primary switch 160 to close substantially when the second duty-cycle signal enters its respective first state, and to cause primary switch 160 to open

substantially when the second duty-cycle signal enters its respective second state. Additionally, the second control means generates a signal at port 184 to cause auxiliary switch 162 to open substantially when the second duty-cycle signal enters its respective first state, and to close substantially when the second duty-cycle signal enters its respective second state. In a preferred embodiment of the present invention, the signals at ports 183 and 184 are non-overlapping such that switches 160 and 162 are not rendered conductive at the same time.

In a further preferred embodiment of the present invention, the PWM means generates the duty cycles signals such that in each the first state is the pulse state and the second state is the resting state. Additionally, each of the duty-cycle signals further comprises a plurality of consecutive switching periods, each said switching period have a substantially constant time duration T. Each switching period begins when its corresponding duty-cycle signal enters its respective first state from its respective second state, continues when its corresponding duty-cycle signal enters its respective second state from its respective first state, and ends when its corresponding duty-cycle signal next enters its respective first state from its respective second state. Further, the consecutive switching periods of the second duty-cycle signal start substantially one-half of the time duration T after the consecutive switching periods of the first duty-cycle signal start. Stated in another way, the second duty-cycle signal enters its respective first (pulse) state substantially T/2 after the first duty-cycle signal enters its respective first (pulse) state. This phase relationship is shown at the timing legend in FIGURE 3 and in graphs 303 and 301 in FIGURE 5 (the T/2 notation at the start of graph 303). In this way. the PWM means generates the duty cycle signals such that the second duty-cycle signal is phase-shifted by substantially 180 degrees from the first duty-cycle signal.

In a preferred embodiment of the present invention, the duration of the first (pulse) states of the duty cycle signals are substantially the same. In other words, the first and second duty-cycle signals are coordinated to have substantially the same duty-cycle value by the PWM means. This aids in having first converter 120 and second converter 150 equally provide power to output port 102.

Exemplary embodiments of the PWM means, first control means, and second control means are now described in greater detail with reference to an

exemplary control means 180 shown at 400 in FIGURE 7. Control means 400 includes output control ports 401-404 corresponding to output control ports 181-184 of control means 180 shown in FIGURE 3. Control means 400 further includes a power port 405, corresponding to power port 185 of control means 180, an output monitoring port 406, corresponding to port 186 of control 180, for receiving a signal related to the voltage provided to output port 102 of DAC converter 100. Control means 400 further includes input ports 407 and 408, corresponding to ports 187 and 188 of control means 180, each for receiving signals representative of the primary current of converters 120 and 150, respectively. Additionally, control means 400 comprises a pulse width modulation (PWM) means 410, a first control means 470, and a second control means 495. PWM means 410 is for generating a first duty-cycle signal at a port 411 for controlling first converter 120, shown in FIGURE 3, and for generating a second duty-cycle signal at a port 412 for controlling second converter 150. First control means 470 is responsive to the first duty-cycle signal at port 411 and is for operating primary switch 130 and auxiliary switch 132 of first converter 120 in a complementary manner. Likewise, second control means 495 is responsive to the second duty-cycle signal at port 412 and is for operating primary switch 160 and auxiliary switch 162 of second converter 150 in a complementary manner. First control means 470 provides a control signal for primary switch 130 at control port 401 and a control signal for auxiliary switch 132 at control port 402. Second control means 495 provides a control signal for primary switch 160 at control port 403 and a control signal for auxiliary switch 162 at control port 404.

PWM means 410 comprises a dual clock generator 420, a first pulse width controller 450 and associate circuitry, and a second pulse width controller 460 and associated circuitry. In a preferred embodiment of control means 400, each of controllers 450 and 460 comprises an AS3843 current mode PWM controller manufactured by Astec Semiconductor. Dual clock generator 420 provides two anti-phase clock signals at two terminals 421 and 422, respectively, which are for driving the two controllers 450 and 460. The anti-phase clock signals are phase shifted with respect to one anther by substantially 180°. Controller 450 is responsive to the first anti-phase clock at terminal 421, to the signal at port 406, which is related to the output voltage of converter 100, and to

the signal at port 407, which is representative of the primary current of converter 120. In response to these signals, controller 450 generates the first duty-cycle signal at port 411 so as to maintain the output voltage of DAC converter 100 near its nominal value. Specifically, controller 450 begins the pulse of the first duty cycle signal in response to the clock signal at terminal 421 and ends the pulse in response to the signals representative of the output voltage and primary current of converter 120.

Controller 460 is responsive to the second anti-phase clock signal at terminal 422, to the signal at port 408, which is representative of the primary current of converter 150, and to a signal generated by controller 450 (provided by the "COMP" pin), which is described in greater detail below. In response to these signals, controller 460 generates the second duty-cycle signal at port 412. Specifically, controller 460 begins the pulse of the second duty cycle signal in response to the clock signal at terminal 422 and ends the pulse in response to the signal provided by controller 450 and to the signal representative of the primary current of converter 150. Since the pulse state of each of the duty cycle signals is initiated in response to its respective clock signal and since the clock signals are phase shifted with respect to one anther by substantially 180° (*i.e.*, in anti-phase), the first and second duty cycle signals are phase shifted with respect to one anther by substantially 180°.

PWM means 410 further includes an internal power supply 415 for providing a low level supply of approximately 12 volts at a terminal 418 to power the various components of PWM means 410 and control means 470 and 495. Internal supply 415 comprises an input port 416 coupled to port 405 for receiving a source of power from the input supply, a ground terminal 417 for providing a ground reference for control means 400, and a power terminal 418 for supplying 12 volts to the various components of means 410, 470, and 495. Ground terminal 417 is preferably coupled to the secondary-side grounds of converters 120 and 150 and to the secondary output ground at output port 102 of DAC converter 100, as shown in FIGURE 3. As such, the secondary outputs of converters 120 and 150 and the circuitry of control means 400 share the same ground. This allows control means 400 to directly sense the voltage at output port 102 of DAC converter 100 without the need for an optocoupler device.

Internal supply 415 preferably comprises a self-oscillating flyback converter, including a power transformer having a primary winding coupled to the input supply at port 405 and a secondary winding coupled between terminals 417 and 418. This power transformer facilitates a ready isolation of the secondary ground at terminal 417 from the input supply at port 405. Internal supply 415 need only supply the amount of current required by the components of control means 400, which is typically less than 0.1 A. The construction of such flyback converters for internal supply 415 are well known in the art, and a detailed explanation thereof is not necessary in order to understand the present invention and to enable one of ordinary skill in the art to make and use the same.

The two anti-phase clocks generated at terminals 421 and 422 by dual clock generator 420 are designated as Φ_1 and Φ_2, respectively. Each of the clock signals Φ_1 and Φ_2 preferably has a first logic state of approximately zero volts and a second logic state of preferably approximately 2.5 volts, and each of the clock signals alternates between its respective first and second states. Additionally, each of the clock signals Φ_1 and Φ_2 has a switching cycle period T of approximately 2.0 microseconds and a duty-cycle of .75 (75%), with the first state being the pulsed state. Also, as indicated above, clock signals Φ_1 and Φ_2 are phase shifted with respect to one anther by substantially 180°, or equivalently, offset in time by one-half of a switching cycle period (T/2 = 1.0 microseconds). Each of the clock signals Φ_1 and Φ_2 are shown as a function of time by a timing diagram 500 in FIGURE 8 in respective timing graphs 505 and 506 of timing diagram 500. Timing diagram 500 also shows a number of additional signals generated by PWM means 410 which will aid in explaining the generation of Φ_1, Φ_2, and the first and second duty cycle signals at ports 411 and 412. These additional signals are shown at timing graphs 501-504, and 507-512.

For generating clock signals Φ_1 and Φ_2, dual clock generator 420 comprises a conventional crystal oscillator for generating a base clock signal, and a D-type flip-flop 430 which is responsive to the base clock and is configured as a toggle flip-flop. Flip-flop 430 includes a clock port "CK" which is coupled to the base clock signal, a data input port "D", an output "Q" and a complementary output "Q\" coupled back to the D input. Flip-flop 430 provides two anti-phase signals at the Q and Q\ outputs, which switch at half the switching frequency of

the base clock signal. Dual clock generator further comprises two logic OR gates for digitally OR-ing the base clock signal with each of the anti-phase signals of flip-flop 430. One OR gate includes two rectifiers 431-432 and two resistors 435-436 and the other OR gate includes two rectifiers 433-434 and two resistors 437-438.

The crystal oscillator includes a crystal 426, a first inverter 424, and a second inverter 429. Crystal 426 is preferably a 1.0 MHz crystal and is coupled between the input and output of first inverter 424, which is preferably a Schmitt-trigger CMOS inverter. A 1 M-ohm resistor 425 is also coupled between the input and output of inverter 424 and is for biasing inverter 424 near the middle of its gain curve characteristic. Additionally, a capacitor 427 of approximately 33 pF is coupled to the input of inverter 424 and a second capacitor 428 of approximately 33 pF is coupled to the output of oscillator 424. With this configuration, a substantially square wave is produced at the output of inverter 424. This output is designated as "OSC" in FIGURE 7 and is shown in a timing graph 501 in FIGURE 8. Second inverter 429 serves to isolate the crystal oscillator from the remaining circuitry of clock generator 420. The input of second inverter 429 is coupled to the "OSC" output. The output of second inverter 429 is the base clock signal and is provided to the clock input of D flip-flop 430 and to the anodes of rectifiers 431 and 434. The output of inverter 429 is designated as "CK" in FIGURE 7 and is shown in a timing graph 502 of FIGURE 8.

As indicated above, the base clock signal at the output of inverter 429 is coupled to the clock input of flip-flop 430. Additionally, the complementary output Q\ is coupled to the data input D. With this configuration, as known in the digital art, the output Q of flip-flop 430 toggles between logic 0 and logic 1 each time the clock input undergoes a logic low-to-high transition. The Q output of flip-flop 430 is shown in a timing diagram 503 of FIGURE 8. The toggle action of the output with respect to the clock input may be seen by comparing timing graphs 502 and 503. The output Q\ of flip-flop 430 is the complement of the Q output of flip-flop 430. The complementary output is shown in a timing graph 504 in FIGURE 8.

The Q output flip-flop 430 is coupled to the anode terminal of rectifier 432, which is a first input of the two-input OR gate formed by rectifiers 431 and 432 and resistors 435 and 436. The second input of this OR gate is provided by the anode of rectifier 431, which is coupled to the base clock (output of inventer 429). The output of this OR gate is coupled to terminal 421 and provides the first clock signal Φ_1 thereto. Resistors 435 and 436 are coupled in series to provide the "pull-down resistor" for the OR gate. One terminal of resistor 435 is coupled to terminal 421 and the other terminal is coupled to each of the cathode terminals of rectifiers 431 and 432. One terminal of resistor 436 is coupled to ground and the other terminal is coupled to terminal 421. As such, the output of the OR gate is generated across resistor 436 and is logic high whenever the base clock or the Q output of flip-flop 430 is high. Each of resistors 435 and 436 preferably has a resistance value of 470 ohms. With these values, the first clock signal Φ_1 has a logic high value of approximately 2.5 volts whenever the clock output of inventer 429 or the Q output of flip-flop 430 is logic high. This is more fully shown in FIGURE 8 by logically OR-ing timing graphs 502 and 503 to obtain the timing graph 505 for the Φ_1 clock signal at terminal 421.

In a similar manner, the Q\ output of flip-flop 430 is coupled to the anode terminal of rectifier 433, which is a first input of the two-input OR gate formed by rectifiers 433 and 434 and resistors 437-438. The second input of this OR gate is provided by the anode of rectifier 434, which is coupled to the base clock (output of inventer 429). The output of this OR gate is coupled to terminal 422 and provides the second clock signal Φ_2 thereto. Resistors 437 and 438 are coupled in series to provide the "pull-down resistor" for the OR gate. One terminal of resistor 437 is coupled to terminal 422 and the other terminal is coupled to each of the cathode terminals of rectifiers 433 and 434. One terminal of resistor 438 is coupled to ground and the other terminal is coupled to terminal 422. As such, the output of the OR gate is generated across resistor 438 and is logic high whenever the base clock or the Q\ output of flip-flop 430 is high. Each of resistors 437 and 438 preferably has a resistance value of 470 ohms. With these values, the second clock signal Φ_2 has a logic high value of approximately 2.5 volts whenever the clock output of inventer 429 or the Q\ output is logic high.

This is more fully shown in FIGURE 8 by logically OR-ing timing graphs 502 and 504 to obtain the timing graph 506 for the Φ_2 clock signal.

As indicated previously, each of controllers 450 and 460 comprises a current mode pulse width modulator, preferably an AS3843 PWM controller manufactured by Astec Semiconductor. Each of controllers 450 and 460 includes a V_{CC} pin for receiving a source of power at approximately 10 volts, a ground pin GND for receiving a ground reference potential of zero volts, and R/C clock pin for receiving its respective clock signal (Φ_1 or Φ_2), a V_{FB} terminal for receiving a signal representative of the output voltage of the converter (DAC converter 100), a COMP compensation terminal for providing a compensation signal to be fed back to the V_{FB} pin, an I_S current sense pin for receiving a voltage related to the output inductor current (or primary current), and an output pin OUT for providing a duty-cycle signal as a function of the signals present on the R/C, V_{FB}, COMP, I_S pins. The R/C pin of controller 450 is coupled to terminal 421 of dual clock generator 420 for receiving first clock signal Φ_1, and the R/C terminal of controller 460 is coupled to terminal 422 for receiving the second clock signal Φ_2. Additionally, the V_{CC} pins for each of the controllers 450 and 460 is coupled to power terminal 418 of internal supply 415, and each of the ground pins is coupled to ground terminal 417 of internal supply 415. The OUT pin of controller 450 provides the first duty-cycle signal at port 411 and the OUT pin of controller 460 provides the second duty-cycle signal at port 412. The first and second duty cycle signals are shown in timing graphs 507 and 508, respectively, of FIGURE 8, and are designated as S_1 and S_2, respectively, in FIGURES 7 and 8. Each of the remaining pins, COMP, V_{FB}, and I_S, are discussed in greater detail below with reference to controller 450.

A voltage proportional to the output voltage of DAC converter 100 is provided to the V_{FB} pin of controller 450. This voltage is generated by a voltage divider comprising two resistors 441 and 442 coupled together at an intermediate node 440. The voltage divider is coupled to port 406 of control means 400 and intermediate node 440 provides the proportional voltage to the V_{FB} pin of controller 450. In a preferred embodiment of control means 400, each of resistors 441 and 442 has a resistance value of 2.2 K-ohms. As such, the voltage at intermediate node 440 is approximately half of the output voltage of DAC

converter 100. Thus, when the value of the output voltage is at its nominal value of five volts, the voltage provided to pin V_{FB} is 2.5 volts.

Within controller 450, the voltage at the V_{FB} pin is compared to an internally generated voltage of 2.5 volts. This comparison is preferably performed by a differential amplifier, often called the error amplifier, having an inverting input coupled to the V_{FB} pin and a non-inverting input coupled to a 2.5 volt reference, which serves to represent the desired output voltage. The output of the error amplifier provides a signal which is related to the difference between the desired output voltage and the measured output voltage. Hence, this voltage is called the error voltage. As the voltage at the V_{FB} pin decreases from 2.5 volts, the error voltage increases, and vice-versa. The error voltage is used to govern the pulse width of the signal S_1 at the output OUT pin. The pulse width increases as this voltage increases and decreases as this voltage decreases. Thus, the pulse width of the first duty-cycle signal at port 411 increases as the sensed output voltage at pin V_{FB} decreases from the reference of 2.5 volts and decreases as the sensed output voltage increases. The increase pulse width causes more power to be delivered to the output, thus increasing the output voltage and thus the voltage at pin V_{FB}. This forms a negative feedback loop which brings the output voltage in regulation to the targeted 5.0 volts.

As is known in the art, such negative feedback control loops often require some form of compensation, or frequency-dependent damping, to ensure that the control loop is stable and does not oscillate in an uncontrolled manner. When the control loop is operated without compensation, the output voltage will typically oscillate at a natural resonant frequency of the control loop. This natural resonant frequency is due to the fact that there is finite delay between the time that the error amplifier causes a correction in the duty cycle of the PWM output signal and the time the converter's filter inductor and output capacitor respond to the corrected duty cycle. In general, the error amplifier can generate an error correction signal to the pulse width modulation faster than the output filter and capacitor can react. A compensation network comprising of two capacitors 451 and 452 and a resistor 453 is connected between the COMP and V_{FB} pins of controller 450. The compensation network is, in turn, coupled between the inverting input of the error amplifier and the output of the error amplifier. The

compensation network feeds back a portion of the output signal to the inverting input so as to slow the operation of the error amplifier down to the response time scale of the output filter and output capacitor. In this way, errant oscillations in the output voltage are mitigated. Exemplary component values for this compensation network are: 2.2 nF for capacitor 451, 150 pF for capacitor 452, and 8.3 K-ohms for resistor 453.

The output voltage of the error amplifier controls the pulse width at the OUT pin in the following manner. The pulse state of the signal S_1 at the OUT pin is initiated by the rising edge at the R/C clock input pin. This is shown at 521 in graph 507 of FIGURE 8. To determine when the pulse state is to end, the error voltage from the error amplifier is compared to the voltage present on the I_S pin. The I_S voltage is proportional to the output filter inductor current of converter 120 during the converter's ON period (*i.e.*, during the pulse state at the OUT pin). In the present invention, this current is sampled by way of the primary circuit current I_{P1}, which is shown at timing graph 308 in FIGURE 5. It has a trapezoidal shape, with the slope of the trapezoid being determined by the input voltage and the inductance of the output filter inductor 140 of first converter 120. This current is preferably sensed by a current transformer (*e.g.*, transformer 135 in FIGURE 3) and coupled to a resistor to convert it to a voltage, which is then provided to the I_S pin. In operation, the output error voltage sets a threshold level which the voltage signal at the I_S pin must reach before controller 450 ends the pulse state of the signal at the OUT pin (i.e. the first duty-cycle signal). However, if the I_S voltage does not reach this threshold before the falling edge of the signal at the R/C pin occurs, controller 450 will terminal the pulsed state at the OUT pin. This limits the maximum duty-cycle of the signal at the OUT pin to be substantially equal to the duty cycle of the signal at the R/C pin, which is preferably 0.75 (75%). The maximum duty cycle for the signal S_1 is shown at 522 in graph 507 of FIGURE 8.

In a preferred embodiment of controller 450, the output error signal is preferably level-shifted and/or scaled before it is compared to the I_S voltage so that it varies between a value of zero and 1V. Additionally, the I_S signal is generated such that it has a range of zero to $-1V$, with the maximum value of $-1V$ corresponding to the maximum allowable current through output filter

inductor 140. In a preferred embodiment of the present invention, the maximum output current for inductor 140 is approximately 23 amperes.

Depending upon the load coupled to the converter, the magnitude of the load current may vary between zero and its maximum value even though the output voltage is at its nominal value. This means that the voltage at the I_s pin may vary between near zero volts and $-1V$ even though the output voltage is at its nominal value. This would appear to be incompatible with the threshold level set by the error amplifier output. However, the negative feedback in the control loop automatically adjusts the threshold level set by the error amplifier to account for changes in the load current. In other words, the threshold level set by the error amplifier is a function of both the output voltage and the average load current.

As known in the art, the comparison of the I_s current with the output error voltage comprises a current mode control loop. Such a current mode control has several advantages. As a first advantage, the current control mode scheme can instantaneously correct for input voltage variations without having the error amplifier swing through large dynamic ranges. This is because the slope of the I_s current is related to the input voltage, decreases (becomes more shallow) as the input voltage decreases from the nominal value and increases (becomes steeper) as the input voltage increases above the nominal value. This allows the duty-cycle to vary within one switching cycle of a change in the input voltage. For example, if the input voltage decreases by a predetermined amount, the slope will also decrease by a predetermined amount, which in turn will extend the duration of the pulse. (*i.e.*, increase the duty-cycle). This in turn increases the amount of power provided to the load within one switching cycle. As a second advantage, the compensation network can be simplified over the conventional voltage mode control loops. This allows for faster response and fewer components.

The voltage signal at the I_s pin of controller 450 is generated in the following manner. A current proportional to the primary circuit current of the first converter 120 is coupled to port 407 of control means 400. This is provided by the current sensing transformer 135 shown in FIGURE 3, as discussed above. This current is typically 1/40th of the current (I_{P1}) flowing in the primary circuit.

This current is fed to a resistor 444, which generates a voltage in proportion to the current provided at port 407. In a preferred embodiment of control means 400, resistor 444 has a value of 5 ohms and is preferably formed by coupling two 10 ohm resistors in parallel. The voltage developed across resistor 444 is then coupled to the I_s pin by way of a resistor 445 and a capacitor 446. Resistor 445 and capacitor 446 filter the voltage developed across resistor 444 such that any leading edge spikes are removed. Such leading edge spikes may cause controller 450 to prematurely end the pulse period of the signal at its OUT pin. In a preferred embodiment, resistor 445 has a value of approximately 200 ohms and capacitor 446 has a value of approximately 100 pF.

As is known in the current art, current control mode schemes have stability problems when the duty-cycle exceeds 50%. This instability is unconditional and occurs regardless of the state of the voltage feedback loop. It is known that by adding a ramp voltage to the voltage generated at resistor 444 this instability can be eliminated. With this added ramp voltage, a current mode controlled converter may operate at duty-cycles greater than 50%. For generating the added ramp voltage, PWM means 410 comprises a ramp generation means including a capacitor 456, a rectifier 458, and three resistors 455, 457, and 459. Resistor 455 and capacitor 456 are coupled in series, and the series combination is coupled between the OUT pin of controller 450 and ground. At the beginning at the pulse period, the voltage at the OUT pin switches from zero volts to approximately 10 volts. This generates an R/C ramp voltage across capacitor 456. This ramp is coupled to the I_s terminal by resistor 457. At the end of the pulse period, the voltage signal at the OUT pin switches from approximately 10 volts to zero volts. Rectifier 458 and resistor 459 discharge the voltage built up on capacitor 456. Rectifier 458 and resistor 459 are coupled in series, and this series combination is coupled between the OUT pin and capacitor 456.

During the pulse period, or ON period, the rising voltage at capacitor 456 injects a current into resistor 445 by way of resistor 457. This injected current causes a voltage drop across resistor 445, which adds to the voltage generated across resistor 444, as indicated above. In this way, the compensation ramp voltage is added to the voltage proportional to the primary circuit current. Preferred values for these components are as follows: resistor

455, 2.2 K-ohm; capacitor 456, 1 nF; resistor 457, 2.2 K-ohms; and resistor 459, 220 ohms. With these values, the ramp voltage across capacitor 456 has a time constant of approximately 1.2 microseconds. With the value of 220 ohms for resistor 445, approximately 1/10th of the ramp voltage at the capacitor 456 is generated across resistor 445. At a 50% duty-cycle and a full load of 20 A per converter, resistor 444 provides approximately 0.4 volts to the I_S pin by the end of the pulse period and resistor 445 provides approximately 0.7 volts to the I_S pin by the end of the pulse period. As is known in the art, the slope of the ramp, as provided across resistor 445, must be greater than 1/2 of the absolute value of the "ripple down slope". The ripple down slope is the slope of the voltage that would be generate across resistor 444 if the output filter inductor's current during the OFF period could be coupled to resistor 444 during the OFF period. Since primary switch 130 of converter 120 is opened during the OFF period, the output filter inductor's current is prevented from being coupled to resistor 444. Nonetheless, given the nominal output voltage, the inductance of filter inductor 140, and the turns ratios of transformers 126 and 135, the ripple down current may be readily calculated.

The functions of the COMP, V_{FB}, and I_S pins for second controller 460 are the same as those of the corresponding pins of controller 450. However, different signals are coupled to the COMP and V_{FB} pins of second controller 460. Specifically, the V_{FB} pin is grounded, which effectively disables the error amplifier of second controller 460. Additionally, the COMP pin of first controller 450 is coupled to the COMP pin of second controller 460, causing the output error signal generated by controller 450 to be used as the output error signal for controller 460. This causes the duty cycles generated at the OUT pins of controllers 450 and 460 to be substantially the same since the same threshold level is used to compare the voltages at the I_S pins of controllers 450 and 460.

The voltage at the I_S pin of controller 460 is generated in the same manner as that for controller 450. Specifically, a current proportional to the primary circuit current of second converter 150 is coupled to port 408 of control means 400. This is provided by the current sensing transformer 165 shown in FIGURE 3, as discussed above. This current is typically 1/40th of the current (I_{P2}) flowing in the primary circuit. This current is fed to a resistor 447, which

generates a voltage in proportion to the current provided at port 408. Resistor 447 preferably has the same resistance as resistor 444. The voltage developed across resistor 447 is coupled to the I_s pin by way of a resistor 448 and a capacitor 449. Resistor 448 preferably has the same resistance as resistor 445 and capacitor 449 preferably has the same capacitance as capacitor 446.

As with controller 450, a ramp voltage from the OUT pin of controller 460 is added to the I_s pin of controller 460 to ensure stable operation for duty cycles above 50%. The ramp generation circuit is substantially the same as that for controller 450 and comprises a capacitor 466, a rectifier 468, and three resistors 465, 467, and 469. These components have substantially the same component values as capacitor 456, rectifier 458, and resistors 455, 457, and 459, respectively.

Having discussed the operation of PWM means 410, the operation of first control means 470 is discussed. As indicated above, first control means 470 is responsive to the first duty-cycle signal S_1 at port 411 and is for operating primary switch 130 and auxiliary switch 132 of first converter 120 in a complementary manner. First control means 470 provides a control signal for primary switch 130 at control port 401 and a control signal for auxiliary switch 132 at control port 402. The control signals at ports 401 and 402 are shown in timing graphs 509 and 510, respectively, of FIGURE 8. First control means 470 comprises a first transistor drive circuit for driving primary switch 130 and a second transistor drive circuit for driving auxiliary switch 132.

The first drive circuit comprises a buffer amplifier 472 having an input and an output, an isolation transformer 474 having a primary winding coupled to the output of amplifier 472 and a secondary winding coupled to port 401, a first coupling capacitor 473 coupled between the output of amplifier 472 and the primary winding of transformer 474, and a second coupling capacitor 475 coupled between the secondary winding of transformer 474 and port 401. Buffer amplifier 472 is responsive to the signal at port 411 and provides the necessary power for driving primary switch 130, transformer 474 provides isolation between the different ground references used by control means 400 and primary switch 130, and coupling capacitors 473 and 475 prevent transformer 474 from becoming saturated. The first drive circuit further comprises a rectifier 476 for clamping the

negative voltage at port 401 and for establishing a "ground" reference potential for port 401. In operation, amplifier 472 provides an output of approximately 10V when signal S_1 is in its pulse state and an output of approximately 0V when signal S_1 is in its resting state. Transformer 474 and capacitors 473 and 475 couple the output of amplifier 472 to port 401.

The first drive circuit further comprises a delay unit coupled between port 411 and the input of amplifier 472. The delay unit includes a resistor 477 and a rectifier 478, each of which are coupled between port 411 and the input of amplifier 472 (cathode of rectifier 478 coupled port 411), and a capacitor 479 coupled between the input of amplifier 472 and ground. This delay unit, along with a similar delay unit in the second transistor drive circuit described below, comprises means for ensuring that the control signals at ports 401 and 402 are not pulsed at the same time, thereby preventing both switches 130 and 132 from conducting at the same time. In response to the leading edge transition of the pulse state for the first duty cycle signal S_1, resistor 477 and capacitor 479 function as an RC delay means which delays the propagation of the leading edge of signal S_1 to the input of amplifier 472. This causes a delay between the leading edge of signal S_1 and the corresponding leading edge of the control signal at port 401. This delay is shown at 525 in graph 509. In response to the falling edge transition of signal S_1, rectifier 478 discharges capacitor 479 with little delay. As such, relatively little delay occurs between the falling edge of signal S_1 and the corresponding falling edge of the control signal at port 401. This is shown at 526 in graph 509 of FIGURE 8.

The second drive circuit comprises an inverting buffer amplifier 482 having an input and an output, an isolation transformer 484 having a primary winding coupled to the output of amplifier 482 and a secondary winding coupled to port 402, a third coupling capacitor 483 coupled between the output of inverting amplifier 482 and the primary winding of transformer 484, and a fourth coupling capacitor 485 coupled between the secondary winding of transformer 484 and port 402. Inverting amplifier 482 is responsive to the signal S_2 at port 412 and provides the necessary power for driving auxiliary switch 132, transformer 484 provides isolation between the different ground references used by control means 400 and auxiliary switch 132, and coupling capacitors 483 and 485 prevent

transformer 484 from becoming saturated. The first drive circuit further comprises a rectifier 486 for clamping the negative voltage at port 402 and for establishing a "ground" reference potential for port 402. In operation, inverting amplifier 482 provides an output of approximately 0V when signal S_1 is in its pulse state and an output of approximately 10V when signal S_1 is in its resting state. Transformer 484 and capacitors 483 and 485 couple the output of amplifier 482 to port 402.

The second drive circuit further comprises a delay unit coupled between port 412 and the input of inverting amplifier 482. The delay unit includes a resistor 487 and a rectifier 488, each of which are coupled between port 412 and the input of amplifier 482 (anode of rectifier 488 coupled port 412), and a capacitor 489 coupled between the input of amplifier 482 and ground. The orientation of rectifier 488 is the reverse of the orientation of rectifier 478. In response to the rising edge transition of the pulse state for the first duty cycle signal S_1, rectifier 488 charges up capacitor 489 relatively quickly. As such, relatively little delay occurs between the rising edge of signal S_1 and the corresponding falling edge of the control signal at port 402. This is shown at 528 in graph 510 of FIGURE 8. In response to the falling edge transition of signal S_1, rectifier 488 is non-conducting and resistor 487 and capacitor 489 function as an RC delay means which delays the propagation of the falling edge of signal S_1 to the input of inverting amplifier 482. This causes a delay between the falling edge of signal S_1 and the corresponding leading edge of the control signal at port 402. This delay is shown at 529 in graph 510.

This delay unit, along the delay unit in the first transistor drive circuit, comprises means for ensuring that the control signals at ports 401 and 402 are not pulsed at the same time, thereby preventing both switches 130 and 132 from conducting at the same time. This may be seen by comparing graphs 509 and 510 shown in FIGURE 8 and by noting the locations of the time delays at 525 and 529.

In a similar manner, second control means 495 shown in FIGURE 7 is responsive to the second duty-cycle signal S_2 at port 412 and is for operating primary switch 160 and auxiliary switch 162 of second converter 150 in a complementary manner. Second control means 495 provides a control signal for

primary switch 160 at control port 403 and a control signal for auxiliary switch 162 at control port 404. The control signals at ports 403 and 404 are shown in timing graphs 511 and 512, respectively, of FIGURE 8. The structure and operation of second control means 495 is substantially identical to those of first control means 470. Therefore, reference is made to the above discussion of first control means 470 for a detailed description of second control means 495.

As mentioned above, this coordination of the control signals at ports 181-184 of control means 180 and at ports 401-404 of control means 400, provides the benefit of substantially reducing the input ripple current at input port 101 and the output ripple current at port 102. This reduction is further explained with reference to timing graphs 305-308 shown in FIGURE 5. In these timing diagrams, the following parameters are taken: a duty cycle of 0.50 (50%); a 4:1 turns ratio for power transformers 126 and 156; a nominal input voltage of 44V, a nominal output voltage of 5V, 40 A output load current (maximum), 20 A for each of converters 120 and 150; a nominal output ripple current of 3 A in each of converters 120 and 150; and a nominal magnetizing ripple current of 0.25 A for each of converters 120 and 150. Graph 305 shows the magnetizing currents I_{M1} and I_{M2} of converters 120 and 150, respectively; graph 306 shows the clamp currents I_{C1} and I_{C2} of converters 120 and 150, respectively; graph 307 shows the output currents I_{L1} and I_{L2} of converters 120 and 150, respectively; and graph 308 shows the primary input currents I_{P1} and I_{P2} of converters 120 and 150, respectively. The currents I_{M1}, I_{C1}, I_{L1}, and I_{P1} for first converter 120 are shown by solid lines in graphs 305-308, and the currents I_{M2}, I_{C2}, I_{L2}, and I_{P2} for second converter 150 are shown by dashed lines in graphs 305-308.

As seen in graph 305, the magnetizing currents I_{M1} and I_{M2} rise during the ON periods of their respective converters and fall during the OFF periods of their respective converters. In a preferred embodiment of the present invention, both magnetizing currents are centered around zero amperes. As indicated above, each of the magnetizing currents I_{M1} and I_{M2} is directed into its corresponding clamp capacitor 134 and 164, respectively, during the OFF period of its converter. This may be seen in graph 306 where I_{C1} is substantially equal to I_{M1} during the OFF period of first converter 120 and where I_{C2} is substantially equal to I_{M2} during the OFF period of second converter 150. As indicated above,

currents I_{C1} and I_{C2} are substantially zero during the ON periods of their respective converters because the auxiliary switches 132 and 162 are not conducting during the respective OFF periods.

The output inductor currents I_{L1} and I_{L2} through inductors 140 and 170, respectively, are shown in graph 307. As seen in graph 307, each of the inductor currents I_{L1} and I_{L2} rises at a substantially uniform rate during the ON period of its converter and falls at a substantially uniform rate during the OFF period of its converter. The rates of increase and decrease (*i.e.*, slopes) of these currents have substantially the same magnitude, which is due to the duty-cycle being at 0.50 (50%). Each of current I_{L1} and I_{L2} are centered about a average D.C. value, which represents the average current delivered to the output by converters 120 and 150, respectively. Due to the substantially 180 degree phase difference in the operation of first converter 120 and second converter 150, current I_{L2} decreases when current I_{L1} increases, and current I_{L2} increases when current I_{L1} decreases. Thus, the ripple in currents I_{L1} and I_{L2} are complimentary to one another and, when combined at output port 102, cancel one another to leave substantially no ripple current at output port 102 for a duty cycle of 0.50 (50%).

The output current at port 102 is designated as current I_{OUT} and is shown in FIGURE 3. The waveform characteristic of I_{OUT} is shown in graph 307 as $I_{OUT}/2$ (dotted line) to better show the cancellation of the ripple components in current I_{L1} and I_{L2}. With this reduction in the output ripple current, the capacitance value and displacement volume of output capacitor 104 may be significantly reduced over that required by a single active clamp forward converter providing the same power capability. (As a comparison, such a single converter would have an output ripple current twice that of current I_{L1}, or that of current I_{L2}.) In the best case of a 50% duty cycle, no output capacitance would be needed to absorb the ripple current. However, as indicated above, the duty-cycle is often varied to compensate for changes in input voltage and output current demand. As the duty cycle of DAC converter 100 is changed from a value of 0.50 (50%), the amount of ripple current increases in proportion to the magnitude of the deviation away from 0.50, *i.e.*, $\propto \| 0.50 - \text{duty cycle} \|$. A more detailed analysis of the output ripple current is given below after the input current I_{P1} and I_{P2} are discussed.

The primary input currents I_{P1} and I_{P2} to converters 120 and 150, respectively, are shown in graph 308 of FIGURE 5. Each of the input currents I_{P1} and I_{P2} rises at a substantially linear rate during the ON period of its corresponding converter, and drops to zero during the OFF period of its corresponding converter. As indicated above, the current I_{P1} during the ON period of converter 120 is equal to the sum of the magnetizing current I_{M1} and to the reflected secondary current, which is substantially equal to $I_{L1}/4$ since the turns ratio of transformer 126 is taken as 4:1. Thus, these components in graphs 305 and 307 add to give I_{P1} in graph 308. During the OFF period, as indicated above, the magnetizing current I_{M1} is directed into clamp capacitor 134, and therefore is not reflected in I_{P1}. Additionally, the secondary current flow during the OFF-period is substantially supported by free-wheeling diode 139, and therefore is not reflected in I_{P1}. Thus, I_{P1} is substantially zero during the OFF periods, as shown in graph 308. A similar analysis applies to primary input current I_{P2} for second converter 150 in relation to its waveform shown in graph 308.

The summation of the input currents I_{P1} and I_{P2} occurs at input port 101, and is designated as I_{MAIN} in FIGURE 3 and graph 308 of FIGURE 5. As can be seen in FIGURE 5, the current I_{MAIN} follows the alternating "ripples" of I_{P1} and I_{P2}. I_{MAIN} comprises a DC component and an AC ripple component, which includes the ripple currents from the magnetizing currents and the ripple currents of the reflected secondary currents. In the exemplary embodiment indicated above, each magnetizing ripple current has a peak-to-peak variation of -0.25 A and each of the secondary ripple currents has a peak-to-peak variation of 3 A. When reflected to the primary circuit with a 4:1 turns ratio, the peak-to-peak variation of each reflected secondary ripple current is 0.75 A. Thus, the peak-to-peak variation of the ripple current of I_{MAIN} in this exemplary embodiment is approximately 1.0 A (0.25 A + 0.75 A). This ripple current is approximately 25% of the maximum DC component of I_{MAIN}, which is -5 A. The AC ripple current of I_{MAIN} is shown in greater detail by a timing diagram 600 in FIGURE 9, which shows at a graph 610 the input ripple currents of a single active clamp forward converter, of DAC converter 100, and of a second embodiment of the DAC converter according to the present invention described in greater detail below. The AC ripple current of I_{MAIN} is shown at 614 in FIGURE 9.

The ripple current for a single active clamp forward converter having the same output power capability as DAC converter 100 is shown at 612 in FIGURE 9. This characteristic may be obtained by multiplying the waveform of I_{P1} shown in graph 308 by 2 (to equalize output power capabilities) and centering the resulting waveform above an average value. The peak-to-peak variation for the input ripple current of the single active clamp forward converter shown at 612 is approximately 11.25 A, which is approximately eleven times the peak-to-peak variation for I_{MAIN} of DAC converter 100, which is -1.0 A.

Timing diagram 600 also shows at a graph 620 the ripple voltages that result from the input ripple currents being applied to a fixed reference capacitor of 1 Farad. To obtain the waveforms for the corresponding ripple voltages, the ripple currents are integrated as a function time over a switching period according to the formula: $V=(1/C)^* \int I\,dt$, C is taken as 1 Farad for a ready basis of comparison. The ripple voltage for the single active clamp converter is shown at 622 in FIGURE 9, and the ripple voltage for DAC converter 100 is shown at 624. (The ripple voltage shown at 622 has been scaled by a factor of one-half so that it may be shown with the other voltages and currents of FIGURE 9.) The ripple voltage shown at 624 has a peak-to-peak value which is roughly forty times smaller than the ripple voltage shown at 622. This is because the peak-to-peak value for the ripple current of DAC converter 100 is roughly 11 times smaller than that for the single active clamp converter, because the ripple current for DAC 100 is triangular whereas the ripple current of the single converter is substantially rectangular, and because the repetition period for the ripple current of DAC converter 100 (*i.e.*, T/2) is one-half that of the single active clamp converter (*i.e.*, T). This means that DAC converter 100 may have, for the same amount of power output capability, an input capacitance which is 2.5% of that required for a single active clamp converter or, conversely, has 2.5% of the input ripple voltage for the same amount of input capacitance.

As indicated above, the output ripple current for DAC converter 100 is essentially zero at a duty cycle of 0.50 (50%). This would be an "infinite" improvement over that of the single active clamp forward converter. However, as indicated above, a finite output ripple current is produced when the duty cycle

varies away from 0.50. An analysis of the output ripple current shows that, in the range of duty cycles from 0.3 to 0.7, the peak-to-peak variation in the ripple current (I_{RPP}) divided by the corresponding variation in a single active clamp forward converter providing the same power capability is given approximately as $(0.88*D+0.25*D^{0.5})$, where $D=\|0.50\text{-duty\_cycle}\|$. In a preferred embodiment of DAC converter 100, the duty cycle ranges between 0.40 (D=0.10) and 0.65 (D=0.15). Thus, taking the larger value of D at 0.15 (duty cycle = 0.65), the maximum output ripple current of DAC converter 100 is only 23% of the output ripple current of a single active clamp forward converter providing the same output power capability.

A further analysis shows that the repetition period of the output ripple current of DAC converter 100 is half that of the single active clamp converter. The combination of halving the repetition period and of reducing the peak-to-peak variation by approximately a factor of 4.3 reduces the amount of ripple voltage at the output by approximately a factor of 8.6. As indicated above with regard to the input ripple current, the amount of output ripple voltage induced by the output ripple current can be calculated by integrating the capacitance formula $I_{RPP} = C_{OUT}\, dV_{RPP}/dt$ to solve for V_{RPP}. Rather than preforming the integration, however, the magnitude of the differential V_{RPP} can be estimated with the formula: $dV_{RPP}= 1/C_{OUT}*I_{RPP}*dt$. Thus, reducing the rippled current I_{RPP} by a factor of 4.3 reduces dV_{RPP} by approximately a factor of 4.3, and reducing the integration time dt by a factor of 2 (by halving the repetition period) further reduces dV_{RPP} by approximately a factor of 2, for a total reduction of approximately 8.6. Thus, for a given output capacitance value, the "noise" at the output of DAC converter 100 is roughly an order of magnitude less than that of the single active clamp forward converter.

In converters 120 and 150 shown in FIGURE 3, the series combination of clamp capacitor 134 and auxiliary switch 132, *i.e.*, the active clamp, is coupled across primary winding 127. However, it may be appreciated that the series combination may be coupled across secondary winding 128, as taught in U.S. Patent No. 4,441,146, issued to Vinciarelli. The coupling of the active clamp in parallel with the secondary winding is demonstrated by active clamp converter 350, shown in FIGURE 6. Converter 350 comprises ports 121a-

125a which corresponding in function to ports 121-125 of first converter 120, shown in FIGURE 3. Converter 350 further comprises the elements 126a - 141a, which correspond in function to elements 126 - 141, respectively, of first converter 120. Further, with an exception of clamp capacitor 134a and auxiliary switch 132a as indicated above, the coupling of the elements of converter 350 is substantially the same as the coupling of elements of first converter 120. It may also be appreciated that the active clamp may also be coupled in parallel to a third winding of power transformer 126, which would be dedicated for the active clamp.

Having thus described a first embodiment of the dual converter according to the present invention, a second embodiment thereof is now described with reference to FIGURE 4 which further reduces the input ripple current by "counter-balancing" the magnetizing currents from the first and second active clamp converters. This second embodiment of the dual active clamp (DAC) converter according to the present invention is shown at 200 in Figure 4. DAC converter 200 comprises an input port 201 for receiving a source of input power to be converted and an output port 202 for providing converted power derived from input port 201. DAC converter 200 further comprises an input capacitor 203 coupled across input port 201 and an output capacitor 204 coupled across output port 202. DAC converter 200 further comprises a first forward active clamp converter 220, a second active clamp forward converter 250, and a control means 280 for coordinating the operation of converters 220 and 250. First converter 220, second converter 250, and control means 280 are each described below in greater detail.

In terms of general function and interconnection, input port 201, output port 202, input capacitor 203, and output port 204 of DAC converter 200 correspond respectively to input port 101, output port 102, input capacitor 103, and output port 104 of DAC converter 100. Additionally, first converter 220, second converter 250, and control means 280 of DAC converter 200 correspond in function to first converter 120, second converter 150, and control means 180 of DAC converter 100 shown in FIGURE 3, respectively. However, as described below, there are substantive internal differences between first converters 220 and 120 and substantive internal differences between second converters 250 and 150.

First converter 220 includes an input port 221 coupled to input port 201 for receiving the source of input power, and output port 222 coupled to output port 202 for providing power to an output load, and control ports 223 and 224 for receiving control signals from control means 280 for controlling the switches of converter 220, each switch being described below in greater detail. Additionally, first converter 220 comprises a power transformer 226 having a primary winding 227 coupled to input port 221 and a secondary winding 228 for coupling power to output port 222. First converter 220 further comprises a current sense transformer 235 for sensing the current flowing into the primary circuit of first converter 220. Sense transformer 235 includes a primary winding 236 having a first terminal coupled to the positive terminal of port 221 and a second terminal coupled to primary winding 227 of power transformer 226. Sense transformer 235 further includes a secondary winding 237 having a first terminal coupled to ground and a second terminal coupled to a current sense output port 225 of first converter 220. Sense transformer 235 provides a current at port 225 which is proportional to that of the current being drawing from the input supply at port 201 by converter 220. The current signal at port 225 is used by control means 280 in controlling the duration switches 130 and 132 are closed, as explained above in the discussion of control means 180 and 400. In a preferred embodiment of the present invention, sense transformer 235 has a turns ratio of 1:40 (primary:secondary).

First converter 220 further comprises a primary switch 230, a clamp capacitor 234, and an auxiliary switch 232. In the preferred embodiment of the present invention, each of switches 230 and 232 comprises a transistor device having a control terminal (gate) and two conduction terminals (source and drain). The gate and source terminals of primary switch 230 are coupled to control port 223 and the gate and source terminals of auxiliary switch 232 is coupled to control port 224. Each of ports 223 and 224 includes two terminals for receiving two signal lines for respective coupling to these gate and source terminals. In a preferred embodiment of the present invention, each of transistor switches 230 and 232 comprises a MOSFET field effect device, preferably with a corresponding integral body diode 231 and 233, respectively. However, it may be appreciated that each of switches 230 and 232 may alternatively comprise other transistor devices, such as bipolar-junction transistors (BJTs).

The ports 221-225 of first converter 220 correspond in function to the ports 121-125 of first converter 120. Additionally, first converter 220 further comprises a node 229, a secondary-side rectifier 238, a free-wheeling rectifier 239, a filter inductor 240, and a second node 241. The elements 226 - 241 of first converter 220 structurally correspond to elements 126 - 141, respectively, of first converter 120. Further, with an exception of clamp capacitor 234 and auxiliary switch 232, the coupling of the elements of first converter 220 is substantially the same as the coupling of elements of first converter 120. In first converter 220, auxiliary switch 232 and clamp capacitor 134 are coupled in series, and the series combination is coupled in parallel with primary switch 230. More specifically, in the embodiments shown in FIGURE 4, the series combination of switch 232 and capacitor 234 is coupled between the drain and source terminals of primary switch 230, and in particular between node 229 and ground.

As with first converter 120 shown in FIGURE 3, designations for various currents are provided for first converter 220. More specifically, the current I'_{M1} represents the magnetizing current through power transformer 226 (referenced to primary winding 227), the current I'_{P1} represents the primary input current into input port 221, and I'_{L1} represents the current flowing through inductor 240 to the load at port 202.

As indicated above, the series combination of auxiliary switch 232 and clamp capacitor 234 of first converter 220 are coupled in parallel with primary switch 230 in contrast to the series combination of auxiliary switch 132 and clamp capacitor 134 of first converter 120, which is coupled in parallel with primary winding 127 of power transformer 126. The parallel coupling with primary switch 230 allows the magnetizing current I'_{M1} during the OFF period for converters 220 to be coupled through to input port 221 and, therefore, show up in the current I'_{P1} during the OFF period of first converter 220. The current I'_{P1} is shown in a graph 309 in FIGURE 5.

As indicated above with regard to first converter 120, the primary input current I_{P1} of converter 120 is equal to the sum of the magnetizing current I_{M1} and the reflected secondary current less the clamp capacitor current I_{C1}, of which the currents I_{M1} and I_{C1} substantially canceled one another in the formation of I_{P1} during the OFF period of converter 120. Therefore, in converter 120 shown

in FIGURE 3, the current I_{P1} is substantially zero during the OFF period (as indicated above, the reflected secondary current is zero during this time). In first converter 220, however, the primary input current I'_{P1} is equal to the sum of the magnetizing current I'_{M1} and the reflected secondary current. As the current I'_{C1} does not form part of the mathematical summation of the input current I'_{P1}, the currents I'_{M1} and I'_{C1} of second converter 220 do not cancel one another in the formation of I'_{P1} during the OFF period of converter 220. Therefore, current I'_{P1} is substantially equal to the current I'_{M1} during the OFF period of converter 220.

Except for these differences between first converters 220 and 120, the operation of first converter 220 is substantially similar to that of first converter 120 shown in FIGURE 3. More specifically, the operation of primary switch 230 and auxiliary switch 232 by control means 280 is substantially similar to that of primary switch 130 and auxiliary switch 132 by control means 180 of first converter 120. Thus, the control signals shown in graphs 301-302 of FIGURE 5 are applicable to first converter 220. Additionally, the process of recycling the magnetizing current I'_{M1} between power transformer 226 and clamp capacitor 234 is substantially similar to that which occurs in first converter 120. As such, the currents I'_{M1} and I'_{C1} are substantially similar in nature to the current I_{M1} and I_{C1} of converter 120 and are shown in graphs 305 and 306 of FIGURE 5. Additionally, the application of voltage to the primary winding is substantially the same due to the substantially similar operation of the primary and auxiliary switches. As such, the application of voltage to the secondary winding and resulting secondary current I'_{L1} flow are substantially the same in first converters 220 and 120. The output inductor current I'_{L1} is shown in graph 307.

A description of the structure and operation of first converter 220 has thus far been given. A similar description is now given for second converter 250. In a preferred embodiment of the present invention, second converter 250 is substantially identical in structure and operation to first converter 220, with one exception being that the switching cycle for converter 250 is substantially different. This difference is substantially similar to the difference in the switching cycle for first converter 120 and second converter 150 and is discussed below in greater detail with reference to the operation of control means 280.

Second converter 250 includes an input port 251 coupled to input port 201 for receiving the source of input power, output port 252 coupled to output port 202 for providing power to an output load, two control ports 253 and 254 for receiving control signals from control means 280 for controlling the switches of converter 250, and a current sense output port 255. Additionally, second converter 250 comprises a power transformer 256 having a primary winding 257 coupled to input port 251 and a secondary winding 258 for coupling power to output port 252. Second converter 250 further comprises a current sense transformer 265 for sensing the current flowing into the primary circuit of second converter 250. Sense transformer 265 includes a primary winding 266 having a first terminal coupled to the positive terminal of port 251 and a second terminal coupled to primary winding 257 of power transformer 256. Sense transformer 265 further includes a secondary winding 267 having a first terminal coupled to ground and a second terminal coupled to current sense output port 255.

Second converter 250 further comprises a primary switch 260, a clamp capacitor 264, and an auxiliary switch 262. In the preferred embodiment of the present invention, each of switches 260 and 262 comprises a transistor device having a control terminal (gate) and two conduction terminals (source and drain). The gate and source terminals of primary switch 260 are coupled to control port 253 and the gate and source terminals of transistor 262 are coupled to control port 254. Each of ports 223 and 224 includes two terminals for receiving two signal lines for respective coupling to these gate and source terminals. Also in a preferred embodiment of the present invention, each of transistor switches 260 and 262 comprises a MOSFET field effect device, preferably with a corresponding integral body diode 261 and 263, respectively. However, it may be appreciated that each of switches 260 and 262 may alternatively comprise other transistor devices, such as bipolar-junction transistors (BJTs).

Second converter 250 further comprises a node 259, a secondary-side rectifier 268, a free-wheeling rectifier 269, a filter inductor 270, and a second node 271. The components 256 - 271 of second converter 250 correspond in function to the components 226 - 241, respectively, of first converter 220. Additionally, the arrangement of these components of second converter 250 is the same as the arrangement of the components of first converter 220. Furthermore,

the basic operation of second converter 250 is the same as that for first converter 220 and the above description of operation for converter 220 is herein applied to describe the operation of second converter 250. As with converter 220, second converter 250 has a magnetizing current I'_{M2} flowing in power transformer 256, a primary input current I'_{P2} flowing in from port 221, a current I'_{C2} flowing into clamp capacitor 264, and an output inductor current I'_{L2} flowing through output filter inductor 270. Reference designations for each of these current is shown in FIGURE 4.

Having thus described the structure and operation of first converter 220 and second converter 250, the operation of control means 280 and the coordination of operating converters 220 and 250 are now described. The structure, function and operation of control means 280 is substantially similar to that of control means 180 previously described. Additionally, an exemplary embodiment of control means 280 is shown by control means 400 in FIGURE 7. For first converter 220, control means 280 includes an output control port 281 coupled to input control port 223 for providing a control signal to primary switch 230, an output control port 282 coupled to input control port 224 for providing a control signal to auxiliary switch 232, and an input port 287 coupled to output port 225 for receiving a signal representative of the primary current of converter 220. Each of ports 281 and 282 comprises two terminals which are coupled to respective terminals of input ports 223 and 224, respective. In a preferred embodiment of DAC converter 200, each of the control signals at ports 281 and 282 appears as a voltage across the terminals of ports 281 and 282, respectively. For second converter 250, control means 280 further includes an output control port 283 coupled to input control port 253 for providing a control signal to primary switch 250, an output control port 284 coupled to input control port 254 for providing a control signal to auxiliary switch 262, and an input port 288 coupled to output port 225 for receiving a signal representative of the primary current of converter 250. Each of ports 283 and 284 comprises two terminals which are coupled to respective terminals of input ports 253 and 254, respectively. In a preferred embodiment of DAC converter 200, each of the control signals at ports 183 and 184 appears as a voltage across the terminals of ports 183 and 184, respectively.

Control means 280 further includes a power port 285 coupled to input port 201 for receiving a source of power and an output monitoring port 286 coupled to output 202 for receiving the voltage provided to port 202. As with control means 180, control means 280 senses the output voltage at port 202 by way of port 286 and respective converter primary currents at ports 187 and 188, and in response thereto, adjusts the duty-cycle of the control signals present on control ports 281-284.

In operation, control means 280 coordinates the operation of first converter 220 and second converter 250 such that the amount of ripple current at input port 201 is minimized. For providing this coordination of control signals at port 281-284, control means 280 further comprises a pulse width modulation (PWM) means for generating a first duty-cycle signal for controlling first converter 220 and a second duty-cycle signal for controlling second converter 250. The generation and properties of the first and second duty-cycle signals of control means 280 are substantially the same as the generation and properties of the first and second duty-cycle signals of control means 180 described earlier. The above discussion regarding control means 180 is therefore incorporated herein by reference.

Control means 280 further comprises a first control means for responsive to the first duty-cycle signal for operating primary switch 230 and auxiliary switch 232 of first converter 220 in a complimentary manner, and a second control means for responsive to the second duty-cycle signal for operating primary switch 260 and auxiliary switch 262 of second converter 250 in a complimentary manner. The first and second control means of control means 280 are substantially identical in function to the first and second control means of control means 180, shown in FIGURE 3. The above discussion regarding control means 180 is therefore incorporated herein by reference. The first control means of control means 280 generates a signal at port 281 for operating primary switch 230, and generates a signal at port 282 for operating auxiliary switch 232. The second control means of control means 280 generates a signal at port 283 for operating primary switch 260, and generates a signal at port 284 for operating auxiliary switch 262.

In a further preferred embodiment of the present invention, the PWM means of control means 280 generates the duty cycles signals such that in each the first state is the pulse state and the second state is the resting state. Additionally, each of the duty-cycle signals further comprises a plurality of consecutive switching periods, each said switching period have a substantially constant time duration T. Each switching period begins when its corresponding duty-cycle signal enters its respective first state from its respective second state, continues when its corresponding duty-cycle signal enters its respective second state from its respective first state, and ends when its corresponding duty-cycle signal next enters its respective first state from its respective second state. Further, the consecutive switching periods of the second duty-cycle signal start substantially one-half of the time duration T after the consecutive switching periods of the first duty-cycle signal start. Stated in another way, the second duty-cycle signal enters its respective first (pulse) state substantially T/2 after the first duty-cycle signal enters its respective first (pulse) state. This phase relationship is shown at the timing legend in FIGURE 4 and in graphs 303 and 301 in FIGURE 5 (the T/2 notation at the start of graph 303). In this way. the PWM means generates the duty cycle signals such that the second duty-cycle signal is phase-shifted by substantially 180 degrees from the first duty-cycle signal.

In a preferred embodiment of the present invention, the duty cycle of the control signals at ports 281 and 283 is nominally set to a value of substantially 0.50 (50%). Additionally, the control signals at ports 281 and 283 are coordinated to have substantially the same duty cycle during operation. In a further preferred embodiment of the present invention, the duty cycle for the control signals at ports 281 and 283 (for the primary switches) ranges between 0.40 and 0.65 about a nominal value of 0.50. As such, the corresponding, complimentary duty cycle for the control signals at ports 282 and 284 (for the auxiliary switches) ranges between 0.60 and 0.35.

As mentioned above, this coordination of the control signals at ports 281-284 provides the benefit of substantially reducing the input ripple current at input port 201 and the output ripple current at port 202. This reduction is further explained with reference to graphs 305-307 and 309 of FIGURE 5, where an exemplary duty cycle of 0.50 (50%) is used. graph 305 shows the magnetizing

currents I'_{M1} and I'_{M2} of converters 220 and 250, respectively; graph 306 shows the clamp currents I'_{C1} and I'_{C2} of converters 220 and 250, respectively; graph 307 shows the output currents I'_{L1} and I'_{L2} of converters 220 and 250, respectively; and graph 309 shows the primary input currents I'_{P1} and I'_{P2} of converters 220 and 250, respectively. As indicated above, the currents I'_{M1}, I'_{C1}, and I'_{L1} for first converter 220 are substantially the same as current I_{M1}, I_{C1}, and I_{L1}, respectively, for first converter 220. These currents are shown by solid lines in graphs 305-306. However, as explained above, the current I'_{P1} for first converter 220 differs from the current I_{P1} for first converter 120 (*c.f.*, the OFF period). Current I'_{P1} is shown by a solid line in graph 309.

For second converter 250, the currents I'_{M2}, I'_{C2}, and I'_{L2} are substantially the same as currents I_{M2}, I_{C2}, and I_{L2}, respectively, for second converter 150. This is because the operation of second converter 250 is phase shifted from that of first converter 220 in substantially the same manner that second converter 150 is phase shifted from that of first converter 120, and because these currents are produced in substantially the same way in each of converters 120, 150, 220, and 250, as discussed above. The currents I'_{M2}, I'_{C2}, and I'_{L2} are shown by dashed lines in graphs 305-306. However, as explained above, the current I'_{P2} for second converter 250 differs from the current I_{P2} for first converter 150 (*c.f.*, the OFF period) for the same reason that current I'_{P1} differs from I_{P1}. Current I'_{P2} is shown by a dashed line in graph 309.

The summation of the input currents I'_{P1} and I'_{P2} occurs at input port 201 and is designated as I'_{MAIN} in FIGURE 4 and in graph 309 of FIGURE 5. As can be seen by comparing graphs 308 and 309 of FIGURE 5, the ripple of current I'_{MAIN} is substantially less than that of the current I_{MAIN} of DAC converter 100. This is because the magnetizing current component of I'_{P1} during the OFF period of first converter 220 substantially cancels the magnetizing current component of I'_{P2} during the ON period of second converter 250 and, vice-versa, the magnetizing current component of I'_{P2} during the OFF period of second converter 250 substantially cancels the magnetizing current component of I'_{P1} during the ON period of first converter 250. The ripple current that remains in current I'_{MAIN} is due to the ripple current present in the inductor currents I'_{L1} and I'_{L2}, as reflected to the primary circuit. As discussed above, the inductor currents

I'_{L1} and I'_{L2} are reflected to the primary circuit substantially only during the ON periods of their respective converters, converters 220 and 250. Thus, the rising edge ripples in currents I'_{L1} and I'_{L2} are propagated to I'_{MAIN}. Using the component values listed in TABLE I and a peak-to-peak value of 3 A for the output ripple current of each converter 220 and 250, the peak-to-peak value of the output ripple current as reflected in I'_{MAIN} of DAC converter 200 is ~0.75 A. This is 0.25 A less than the ripple current of I_{MAIN} for DAC converter 100, which is 1.0 A, and represents a 25% reduction in the amount of input ripple current.

Because that the peak-to-peak range in the currents I'_{L1} and I'_{L2} of DAC converter 200 is larger than that in the currents I_{L1} and I_{L2} of DAC converter 100, it is counter-intuitive that the input current I'_{MAIN} of DAC converter 200 has less ripple current than input current I_{MAIN} of DAC converter 100. This is also counter-intuitive because the I'_{L1} and I'_{L2} waveforms each have a greater structural variation (*i.e.*, more line segments per switching cycle) than the I_{L1} and I_{L2} waveforms, respectively. For these reasons, it would not be apparent to one of ordinary skill in the art that the differences between DAC converters 100 and 200 would lead to such a further reduction in the input ripple current of DAC converter 200.

The effects of this further reduction is discussed with reference to FIGURE 9. As previously discussed, FIGURE 9 shows a timing diagram 600 showing the input ripple current of a single active clamp forward converter at 612, and the input ripple current of DAC converter 100 at 614. Timing diagram 600 also shows at a graph 620 the input ripple voltages at 622 and 624 that result from these input ripple currents being applied to a fixed reference capacitor of 1 Farad. The input ripple current component of I'_{MAIN} is shown at 616 in FIGURE 9. As seen, I'_{MAIN} has a peak-to-peak variation which is roughly 75% that of I_{MAIN} shown at 614. The corresponding input ripple voltage is shown at 626 in FIGURE 9, and is calculated in the same manner as that for DAC converter 100. The peak-to-peak variation in the input ripple voltage for DAC converter 200 is roughly 75% that of DAC converter 100 and roughly 1/50th that of the single active clamp forward converter. This means that DAC converter 100 may have, for the same amount of power output capability, an input capacitance which is 2% of that

required for a single active clamp converter or, conversely, may have 2% of the output ripple voltage for the same amount of input capacitance.

However, the relative improvement in input ripple current between DAC converter 200 and DAC converter 100 is a function of the ratio of the level of magnetizing current to the level of reflected secondary-side current. In the above examples, the level of magnetizing current was set to be roughly 33% of the reflected secondary-side current. With this, a reduction of −25% is achieved by DAC converter 200 over DAC converter 100. However, when the level of reflected secondary-side current is much larger than the level of magnetizing current, the relative improvement between DAC converters 200 and 100 becomes small, as both DAC converters 100 and 200 provide substantially the same degree of cancellation in the reflected secondary ripple current. However, in cases where the level of magnetizing current is comparable to the level of reflected secondary-side current, the reduction of ripple current by DAC converter 200 is greater.

With regard to the output ripple current for DAC converter 200, since the inductor currents I'_{L1} and I'_{L2} of DAC converter 200 are substantially similar to the inductor currents I_{L1} and I_{L2} of DAC converter 100, the output ripple current characteristics for DAC converter 200 are substantially similar to those of DAC converter 100. That is, substantially no output ripple current at a duty cycle of 0.50 and increasing output ripple current as the duty cycle varies from the 0.50 value. The output current for DAC converter 200 is designated as I'_{OUT}, and is shown in FIGURE 4 at port 202. Additionally, the waveform of I'_{OUT} is shown via the waveform for $I'_{OUT}/2$ in graph 307 of FIGURE 5.

Various preferred embodiments of DAC converters 100 and 200 suitable for telephone equipment and the like are now described. These embodiments comprise the component values listed in TABLE I and are switched at a frequency of approximately 500kHz. In one such embodiment, the nominal input voltage is 44V, the nominal output voltage is 5V, the transformer turns ratio is 4:1, and the input voltage restricted to a narrow range of ±20% around 44V, which would be the range of 35V to 53V. From equation 2 above, the duty-cycle is approximately 0.63 (63%) for an input voltage of 35V and approximately 0.41 (41%) for an input voltage of 53V. In a further embodiment to this, the input voltage is restricted to a narrow range of ±10% from 44V, which would be the

range of 39.6V to 48.4V. The duty cycles at 39.6V and 48.4V for an output voltage of 5V are 0.56 (56%) and 0.45 (45%), respectively.

In another such preferred embodiment, the nominal input voltage is 48V, the nominal output voltage is 5.5V, the transformer turns ratio is 4:1, and the input voltage restricted to a narrow range of ±20% around 48V, which would be the range of 38V to 58V. As before, the duty-cycle is approximately 0.63 (63%) for an input voltage of 38V and approximately 0.41 (41%) for an input voltage of 58V. In still another such preferred embodiment, the nominal input voltage is 48V, the nominal output voltage is 6.3V, and the transformer turns ratio is 7:2.

The input ripple current of a 44VDC-to-5VDC DAC converter 100 with the above parameters (*cf.* TABLE I) is now compared with a standard push-pull converter, which is shown at 700 in FIGURE 10. Push-pull converter 700 comprises a power transformer T_1 having two primary windings and two secondary windings, two primary switches SW_1 and SW_2, and input capacitor C_{IN}, two secondary diodes D_1 and D_2, an output filter inductor L_{OUT}, and an output capacitor C_{OUT}, interconnected as shown in FIGURE 10. The nominal duty cycle for each switch SW_1 and SW_2 is 30%, the target output voltage is 5V, and the nominal input voltage is 46V. A secondary voltage loss of 0.5V is assumed for diodes D_1 and D_2.

The input ripple currents for DAC converter 100 and for push-pull converter 700 each create corresponding input ripple voltages at their respective input capacitors. A comparison between these input ripple voltages is shown at a graph 800 in FIGURE 11, where an input capacitance value of 1.0uF is taken for both converters. Graph 800 comprises an X-axis 801 displaying the input voltage (in volts) and a Y-axis displaying the input ripple voltage (also in volts). The input ripple current for push-pull converter 700 is shown at 810 as a function of input voltage and the input ripple current of DAC converter 100 is shown at 820 as a function of input voltage. For push-pull converter 700, the nominal operating point is shown at 814, where the input voltage is 46V and the duty cycle is 0.30 (30%). The ±20% input voltage points are shown at 812 and 816, where the duty cycle has a value of 0.25 (25%) and 0.37 (37%), respectively. Likewise, for push-DAC converter 100, the nominal operating point is shown at 822, where the

input voltage is 44V and the duty cycle is 0.50 (50%). The ±20% input voltage points are shown at 824 and 826, where the duty cycle has a value of 0.63 (63%) and 0.415 (41.5%), respectively. As can be seen in FIGURE 11, the input ripple voltage for DAC converter 100 is less then the input ripple voltage for push-pull converter. At the -20% input voltage point, the input ripple voltage for DAC converter 100 is more than 35% less. At the +20% input voltage point, the input ripple voltage for DAC converter 100 is approximately 61% less.

While the present invention has been particularly described with respect to the illustrated embodiments, it will be appreciated that various alterations, modifications and adaptations may be made based on the present disclosure, and are intended to be within the scope of the present invention. While the invention has been described in connection with what is presently considered to be the most practical and preferred embodiments, it is also to be understood that the present invention is not limited to the disclosed embodiments but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the scope of the appended claims.

WHAT IS CLAIMED IS:

1. A dual active clamp forward converter comprising:

an input port for receiving a source of power and an output port for providing power to a load;

a first converter and a second converter, each said converter having a power transformer including a primary winding coupled to said input port and a secondary winding coupled to said output port, a primary switch coupled in series between said primary winding of said power transformer and said input port, and a series combination of an auxiliary switch and a capacitor, said series combination coupled across one of said windings of said power transformer;

means for generating a first duty-cycle signal and a second duty-cycle signal for controlling the switching state of said first converter and said second converter respectively, each of said first and second duty-cycle signals having a first state and a second state and alternating in time between its respective first and second states, said second duty-cycle signal being phase-shifted in time by substantially 180 degrees from said first duty-cycle signal;

a first control means responsive to said first duty-cycle signal for operating the primary switch and the auxiliary switch of said first converter, said first control means causing the primary switch of said first converter to close substantially when said first duty-cycle signal enters its respective first state and causing the primary switch of said first converter to open substantially when said first duty-cycle signal enters its respective second state, said first control means causing the auxiliary switch of said first converter to open substantially when said first duty-cycle signal enters its respective first state and to close substantially when said first duty-cycle signal enters its respective second state; and

a second control means responsive to said second duty-cycle signal for operating the primary switch and the auxiliary switch of said second converter, said second control means causing the primary switch of said second converter to close substantially when said second duty-cycle signal enters its respective first state and causing the primary switch of said second converter to open substantially when said second duty-cycle signal enters its respective second state, said second control means causing the auxiliary switch of said second converter to open substantially when said second duty-cycle signal enters its respective first state and

to close substantially when said second duty-cycle signal enters its respective second state.

2. The dual active clamp converter of Claim 1 wherein each of said first and second duty-cycle signals further comprises a plurality of consecutive switching periods, each said switching period having a substantially constant time duration T, each said switching period beginning when its corresponding duty-cycle signal enters its respective first state from its respective second state, continuing when its corresponding duty-cycle signal enters its respective second state from its respective first state, and ending when its corresponding duty-cycle signal next enters its respective first state from its respective second state.

3. The dual active clamp converter of Claim 2 wherein the consecutive switching periods of said second duty-cycle signal start substantially one-half of said time duration T after the consecutive switching periods of said first duty-cycle signal start.

4. The dual active clamp converter of Claim 2 wherein the ratio of the duration said first duty-cycle signal is in its said first state to the duration of said time duration T is between 0.30 and 0.70, and wherein the ratio of the duration said second duty-cycle signal in its said first state to the duration of said time duration T is between 0.30 and 0.70.

5. The dual active clamp converter of Claim 2 wherein the ratio of the duration said first duty-cycle signal is in its said first state to the duration of said time duration T is between 0.40 and 0.65, and wherein the ratio of the duration said second duty-cycle signal in its said first state to the duration of said time duration T is between 0.40 and 0.65.

6. The dual active clamp converter of Claim 2 wherein the ratio of the duration said first duty-cycle signal is in its said first state to the duration of said time duration T is substantially the same as the ratio of the duration said second duty-cycle signal in its said first state to the duration of said time duration T.

7. The dual active converter of Claim 2 wherein said means for generating said first and second duty cycle signals comprises means for regulating the output voltage at said output port within a range around a predetermined target value, wherein the voltage at said input port is at a nominal value when the

voltage at said output port is substantially at said predetermined target value, and wherein the ratio of the duration said first duty-cycle signal is in its said first state to the duration of said time duration T is substantially 0.50 and the ratio of the duration said second duty-cycle signal in its said first state to the duration of said time duration T is substantially 0.50 when said input voltage is at its nominal value and the voltage at said output port is at said predetermined target value.

8. The dual active converter of Claim 1 wherein the series combination of the auxiliary switch and the capacitor of said first converter is coupled across the primary winding of the power transformer of said first converter, and wherein the series combination of the auxiliary switch and the capacitor of said second converter is coupled across the primary winding of the power transformer of said second converter.

9. The dual active converter of Claim 1 wherein the series combination of the auxiliary switch and the capacitor of said first converter is coupled across the secondary winding of the power transformer of said first converter, and wherein the series combination of the auxiliary switch and the capacitor of said second converter is coupled across the secondary winding of the power transformer of said second converter.

10. A dual active clamp converter comprising:

an input port for receiving a source of power and an output port for providing power to a load;

a first converter and a second converter, each said converter having a power transformer including a primary winding coupled to said input port and a secondary winding coupled to said output port, a primary switch coupled in series between said primary winding of said power transformer and said input port, and a series combination of an auxiliary switch and a capacitor, said series combination being coupled in parallel with said primary switch;

means for generating a first duty-cycle signal and a second duty-cycle signal for controlling the switching state of said first converter and said second converter respectively, each of said first and second duty-cycle signals having a first state and a second state and alternating in time between its r[illegible] first and second states, said second duty-cycle signal being phase-shift[illegible] by substantially 180 degrees from said first duty-cycle signal;

a first control means responsive to said first duty-cycle signal for operating the primary switch and the auxiliary switch of said first converter, said first control means causing the primary switch of said first converter to close substantially when said first duty-cycle signal enters its respective first state and causing the primary switch of said first converter to open substantially when said first duty-cycle signal enters its respective second state, said first control means causing the auxiliary switch of said first converter to open substantially when said first duty-cycle signal enters its respective first state and to close substantially when said first duty-cycle signal enters its respective second state; and

a second control means responsive to said second duty-cycle signal for operating the primary switch and the auxiliary switch of said second converter, said second control means causing the primary switch of said second converter to close substantially when said second duty-cycle signal enters its respective first state and causing the primary switch of said second converter to open substantially when said second duty-cycle signal enters its respective second state, said second control means causing the auxiliary switch of said second converter to open substantially when said second duty-cycle signal enters its respective first state and to close substantially when said second duty-cycle signal enters its respective second state.

11. The dual active clamp converter of Claim 10 wherein each of said first and second duty-cycle signals further comprises a plurality of consecutive switching periods, each said switching period having a substantially constant time duration T, each said switching period beginning when its corresponding duty-cycle signal enters its respective first state from its respective second state, continuing when its corresponding duty-cycle signal enters its respective second state from its respective first state, and ending when its corresponding duty-cycle signal next enters its respective first state from its respective second state.

12. The dual active clamp converter of Claim 11 wherein the consecutive switching periods of said second duty-cycle signal start substantially one-half of said time duration T after the consecutive switching periods of said first duty-cycle signal start.

13. The dual active clamp converter of Claim 11 wherein the ratio of the duration said first duty-cycle signal is in its said first state to the duration of

said time duration T is between 0.30 and 0.70, and wherein the ratio of the duration said second duty-cycle signal in its said first state to the duration of said time duration T is between 0.30 and 0.70.

14. The dual active clamp converter of Claim 11 wherein the ratio of the duration said first duty-cycle signal is in its said first state to the duration of said time duration T is between 0.40 and 0.65, and wherein the ratio of the duration said second duty-cycle signal in its said first state to the duration of said time duration T is between 0.40 and 0.65.

15. The dual active clamp converter of Claim 11 wherein the ratio of the duration said first duty-cycle signal is in its said first state to the duration of said time duration T is substantially the same as the ratio of the duration said second duty-cycle signal in its said first state to the duration of said time duration T.

16. The dual active converter of Claim 11 wherein said means for generating said first and second duty cycle signals comprises means for regulating the output voltage at said output port within a range around a predetermined target value, wherein the voltage at said input port is at a nominal value when the voltage at said output port is substantially at said predetermined target value, and wherein the ratio of the duration said first duty-cycle signal is in its said first state to the duration of said time duration T is substantially 0.50 and the ratio of the duration said second duty-cycle signal in its said first state to the duration of said time duration T is substantially 0.50 when said input voltage is at its nominal value and the voltage at said output port is at said predetermined target value.

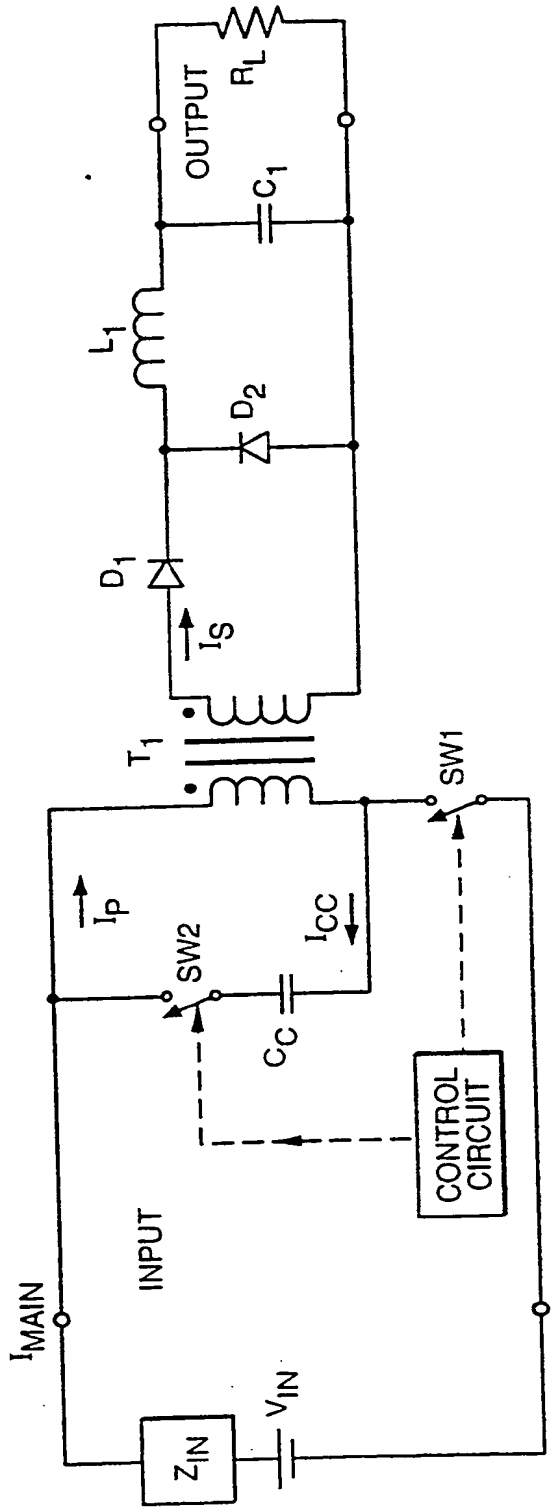


FIG._1
(PRIOR ART)

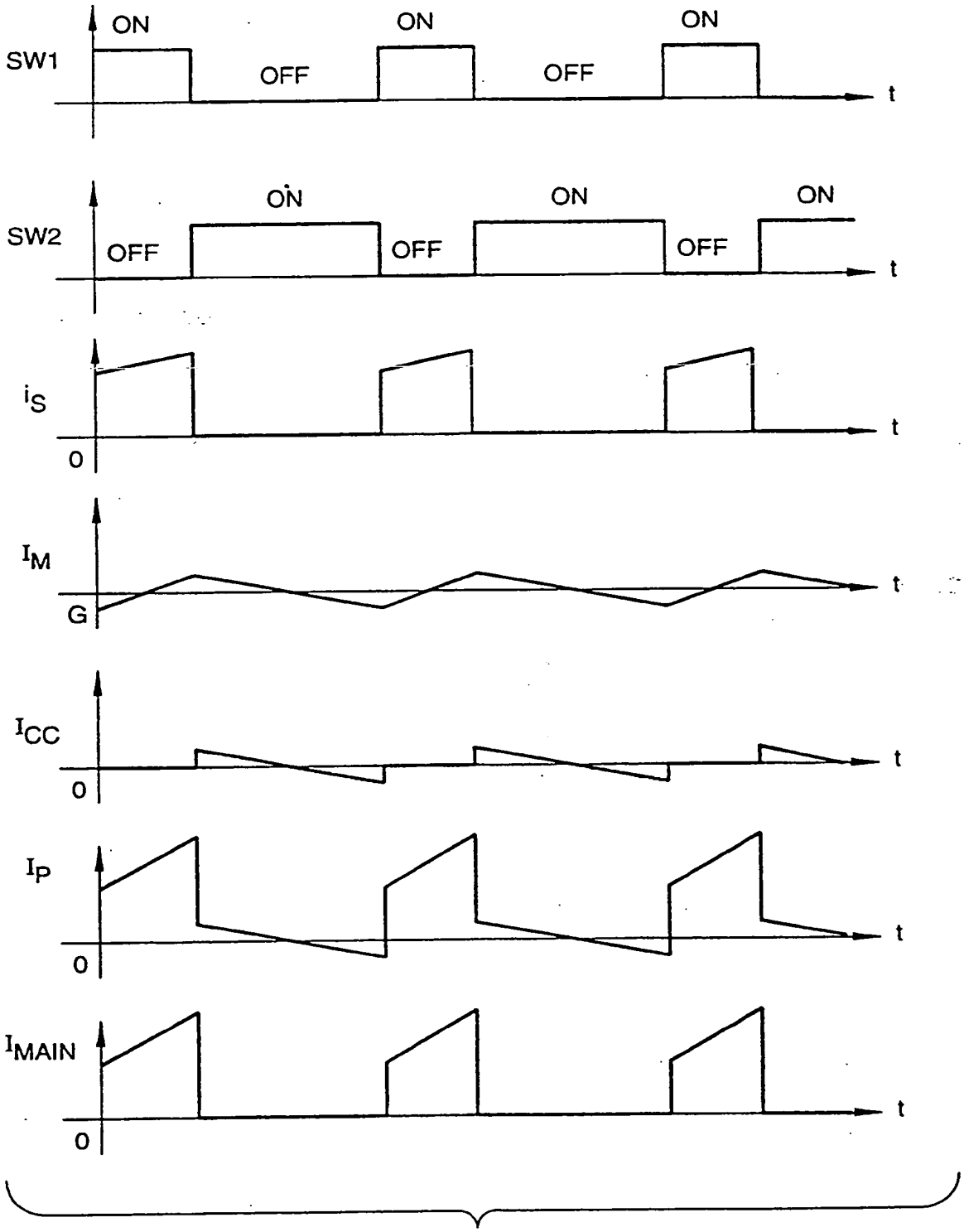
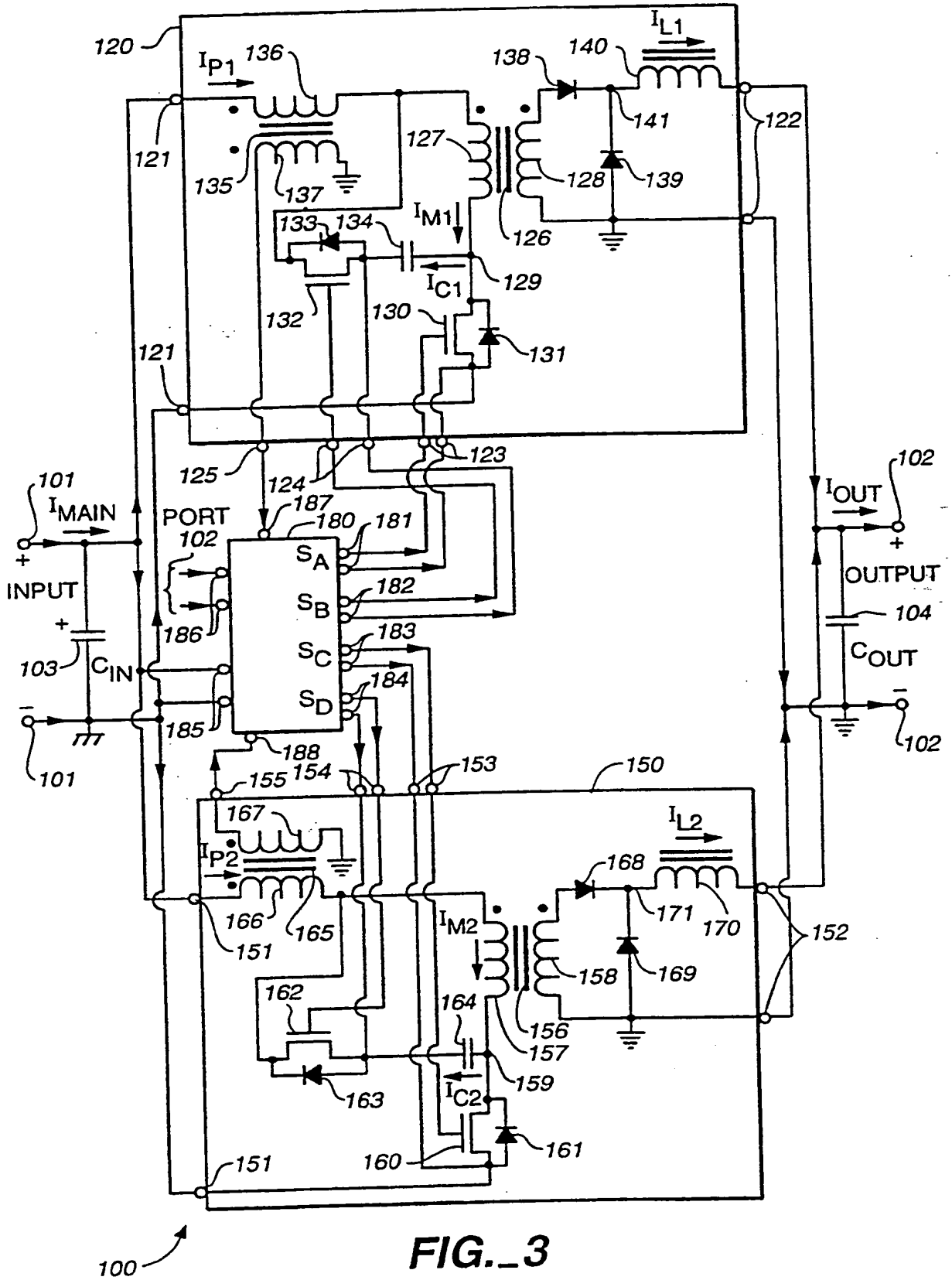


FIG._2
(PRIOR ART)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I_{L1}
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137
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141
122
128
139
I_{M1}
133
134
126
129
I_{C1}
132
130
131
121
123
125
124
187
101
I_{MAIN}
PORT
180
181
102
S_A
S_B
S_C
S_D
182
183
184
186
185
188
INPUT
103
C_{IN}
101
155
154
153
150
167
I_{P2}
I_{L2}
168
166
165
151
I_{M2}
171
170
152
158
169
162
164
156
157
159
163
I_{C2}
161
160
151
100
102
I_{OUT}
OUTPUT
104
C_{OUT}
102

FIG._3

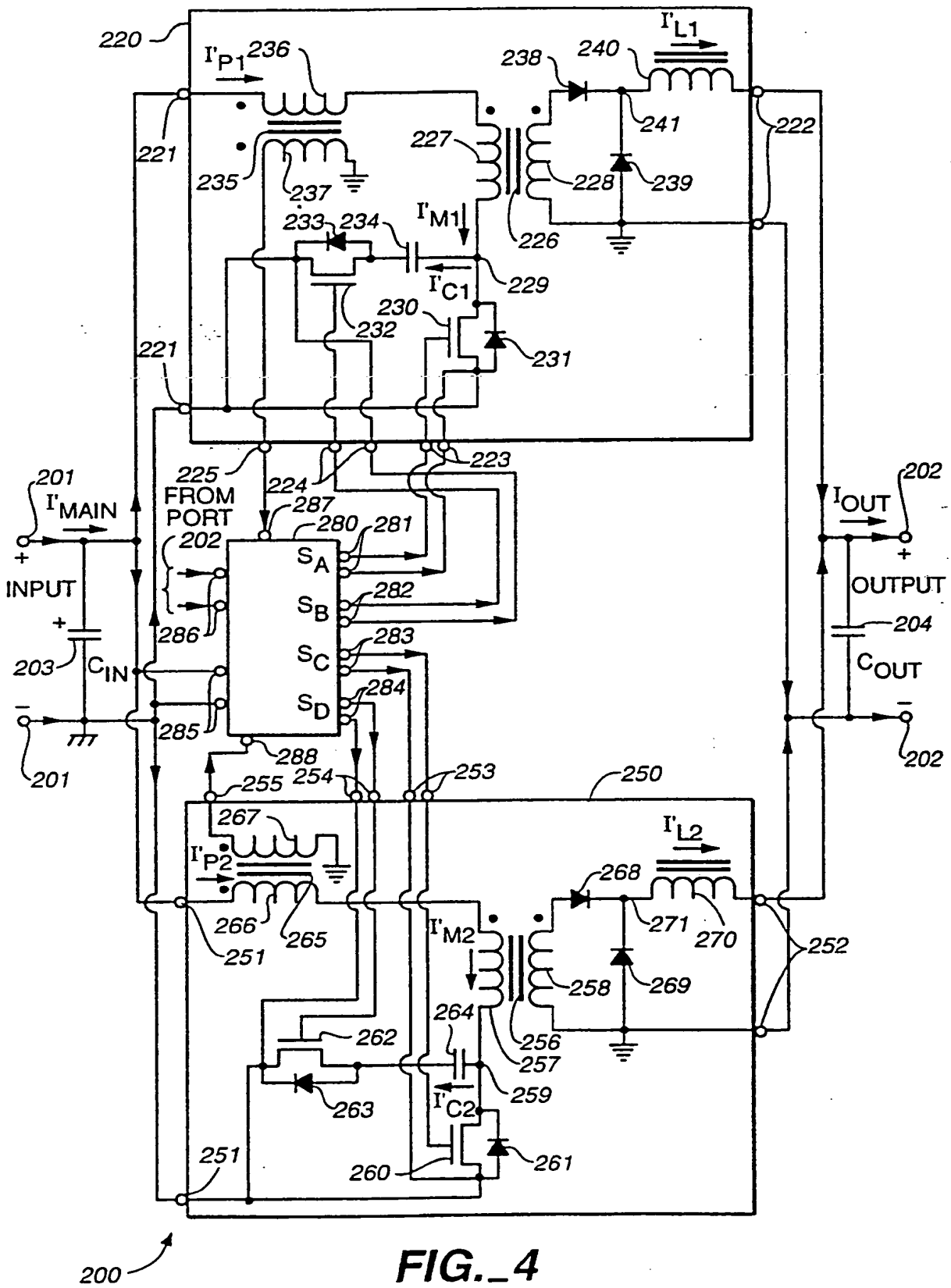

220
I'P1
236
238
240
I'L1
221
235
237
227
241
222
228
239
I'M1
233
234
226
229
I'C1
230
232
231
221
223
225
FROM PORT
224
287
280
281
201
I'MAIN
202
SA
SB
SC
SD
282
283
284
286
INPUT
203
CIN
285
288
255
254
253
250
201
202
IOUT
OUTPUT
204
COUT
202
267
I'P2
I'L2
268
266
265
271
270
251
I'M2
252
258
269
264
262
256
257
259
263
I'C2
251
260
261
200

FIG._4

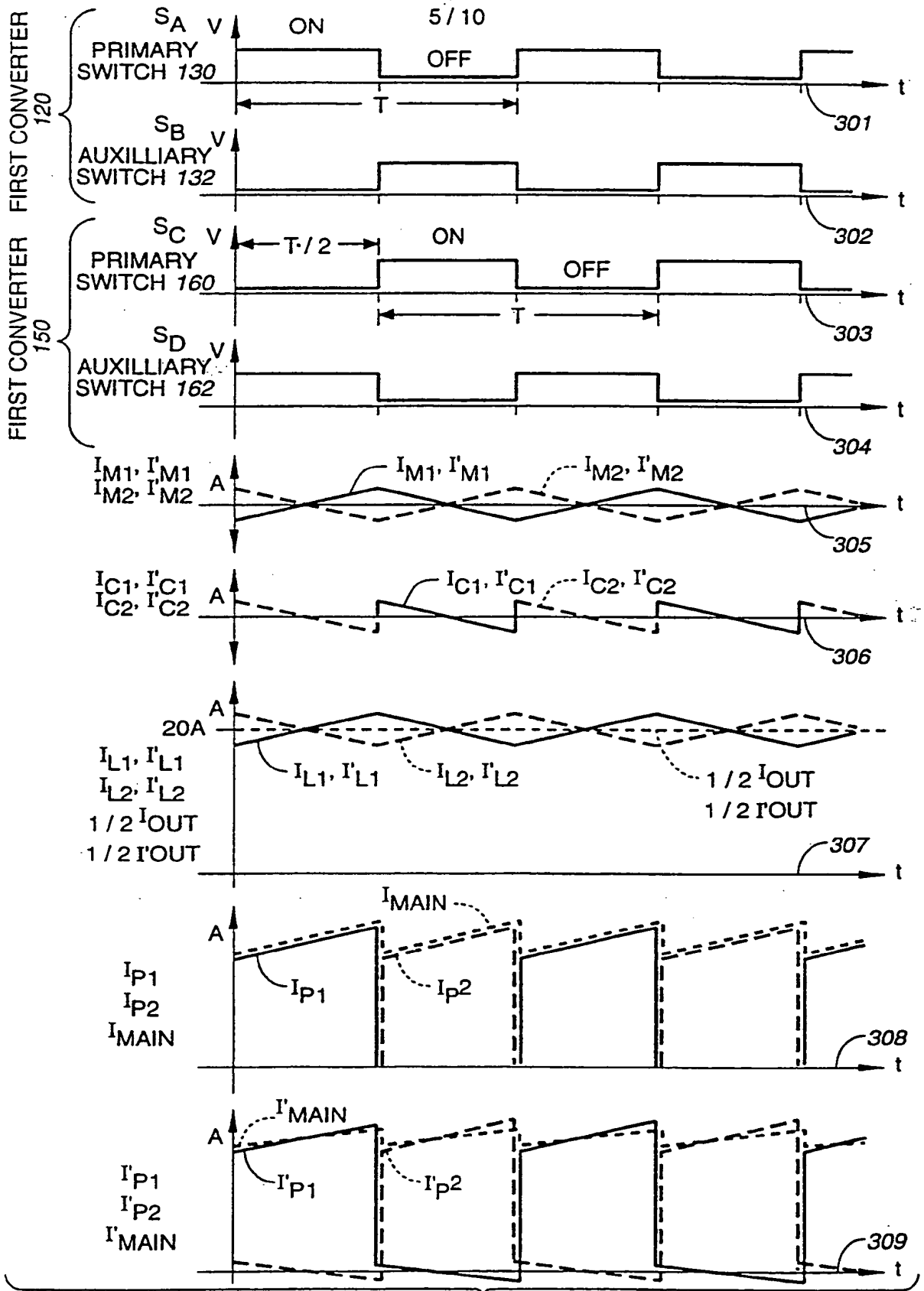
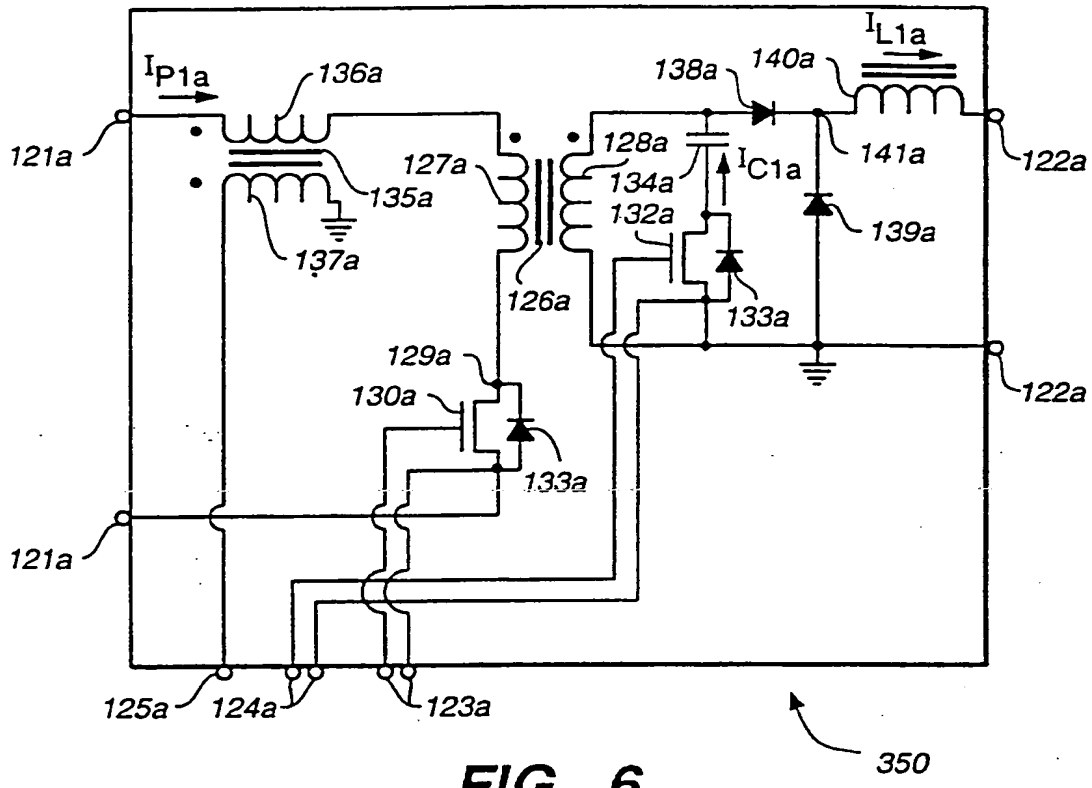

FIRST CONVERTER 120
FIRST CONVERTER 150
S_A V
PRIMARY SWITCH 130
ON
OFF
T
t
301
S_B V
AUXILLIARY SWITCH 132
302
S_C V
T / 2
PRIMARY SWITCH 160
303
S_D V
AUXILLIARY SWITCH 162
304
I_{M1}, I'_{M1}
I_{M2}, I'_{M2}
A
305
I_{C1}, I'_{C1}
I_{C2}, I'_{C2}
306
20A
I_{L1}, I'_{L1}
I_{L2}, I'_{L2}
1 / 2 I_{OUT}
1 / 2 I'_{OUT}
307
I_{MAIN}
I_{P1}
I_{P2}
308
I'_{MAIN}
I'_{P1}
I'_{P2}
309
300

FIG._5


I_{P1a}
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137a
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126a
128a
134a
132a
I_{C1a}
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140a
I_{L1a}
141a
122a
139a
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130a
133a
121a
122a
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124a
123a
350

FIG._6

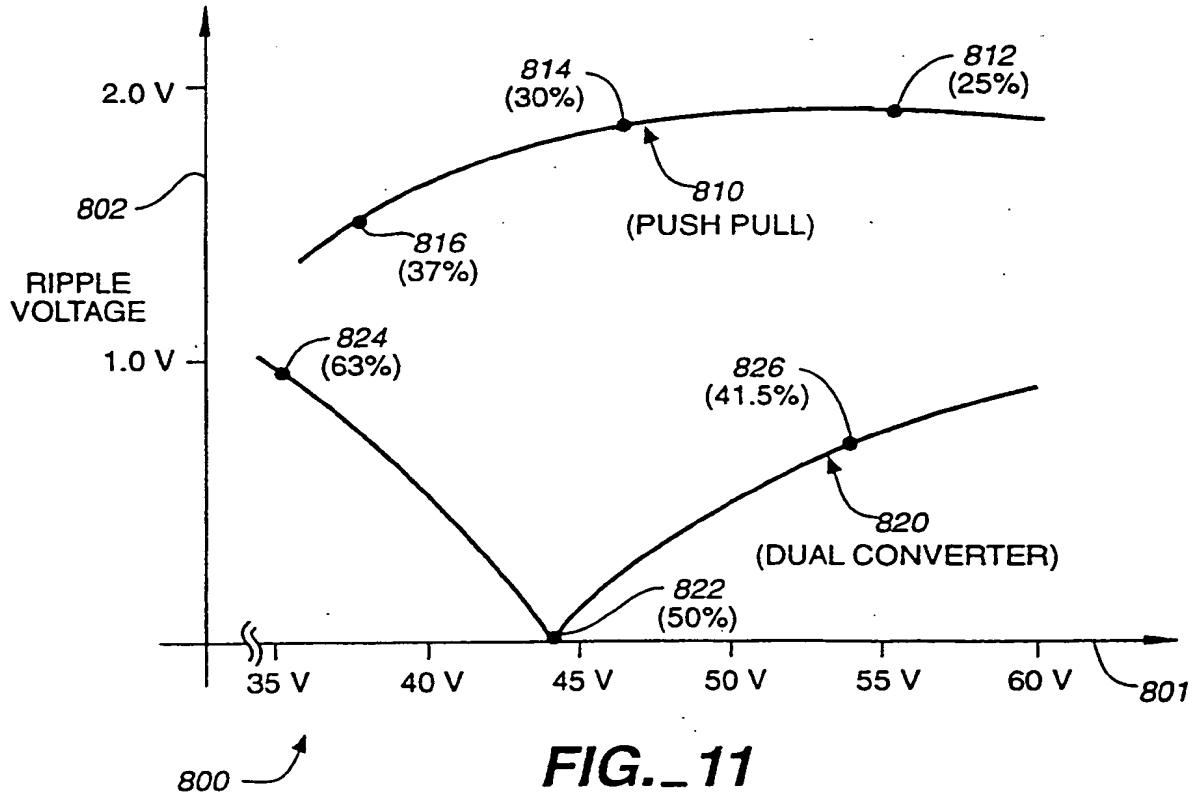
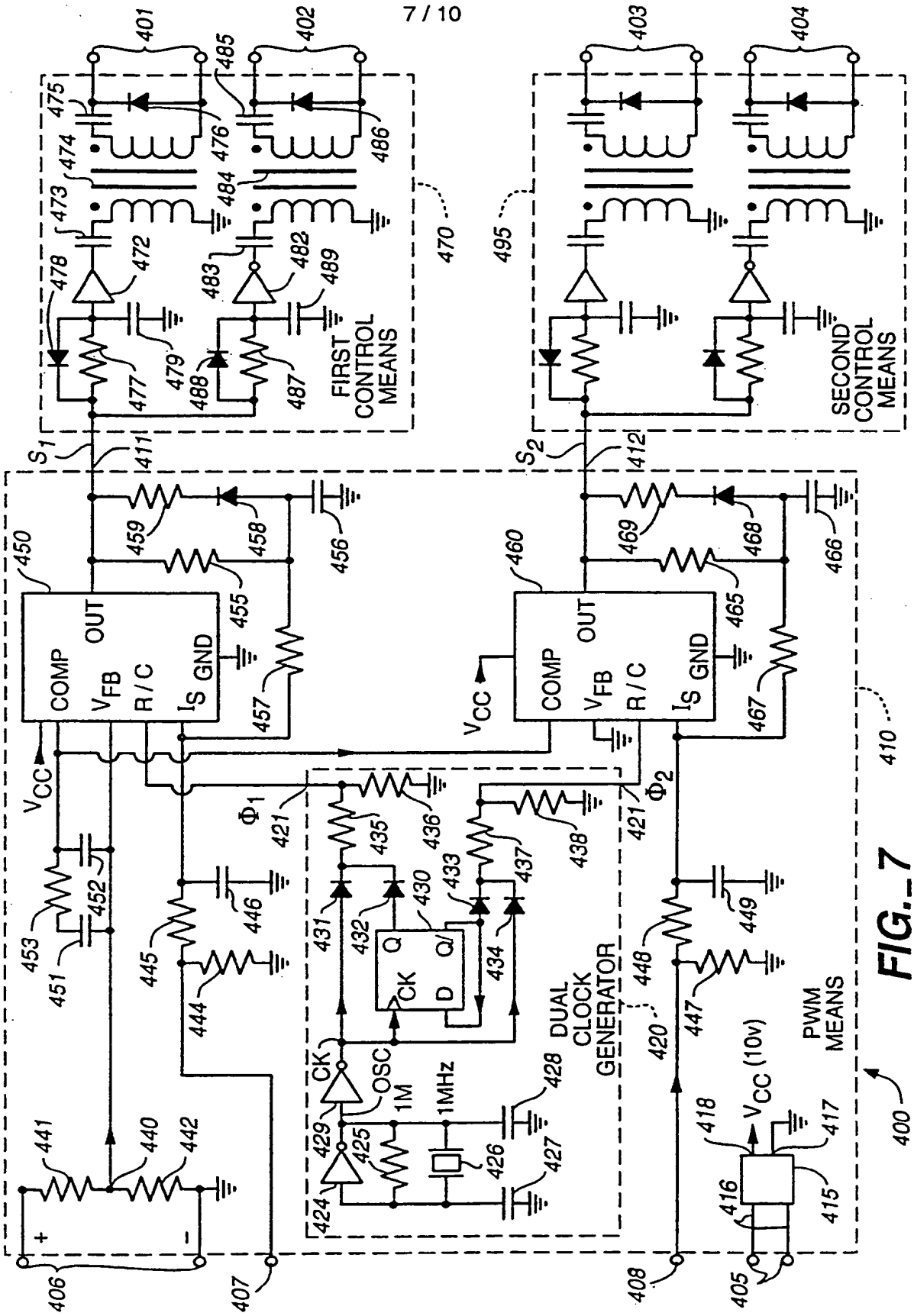

2.0 V
802
RIPPLE VOLTAGE
1.0 V
814 (30%)
812 (25%)
810 (PUSH PULL)
816 (37%)
824 (63%)
826 (41.5%)
820 (DUAL CONVERTER)
822 (50%)
35 V
40 V
45 V
50 V
55 V
60 V
801
800

FIG._11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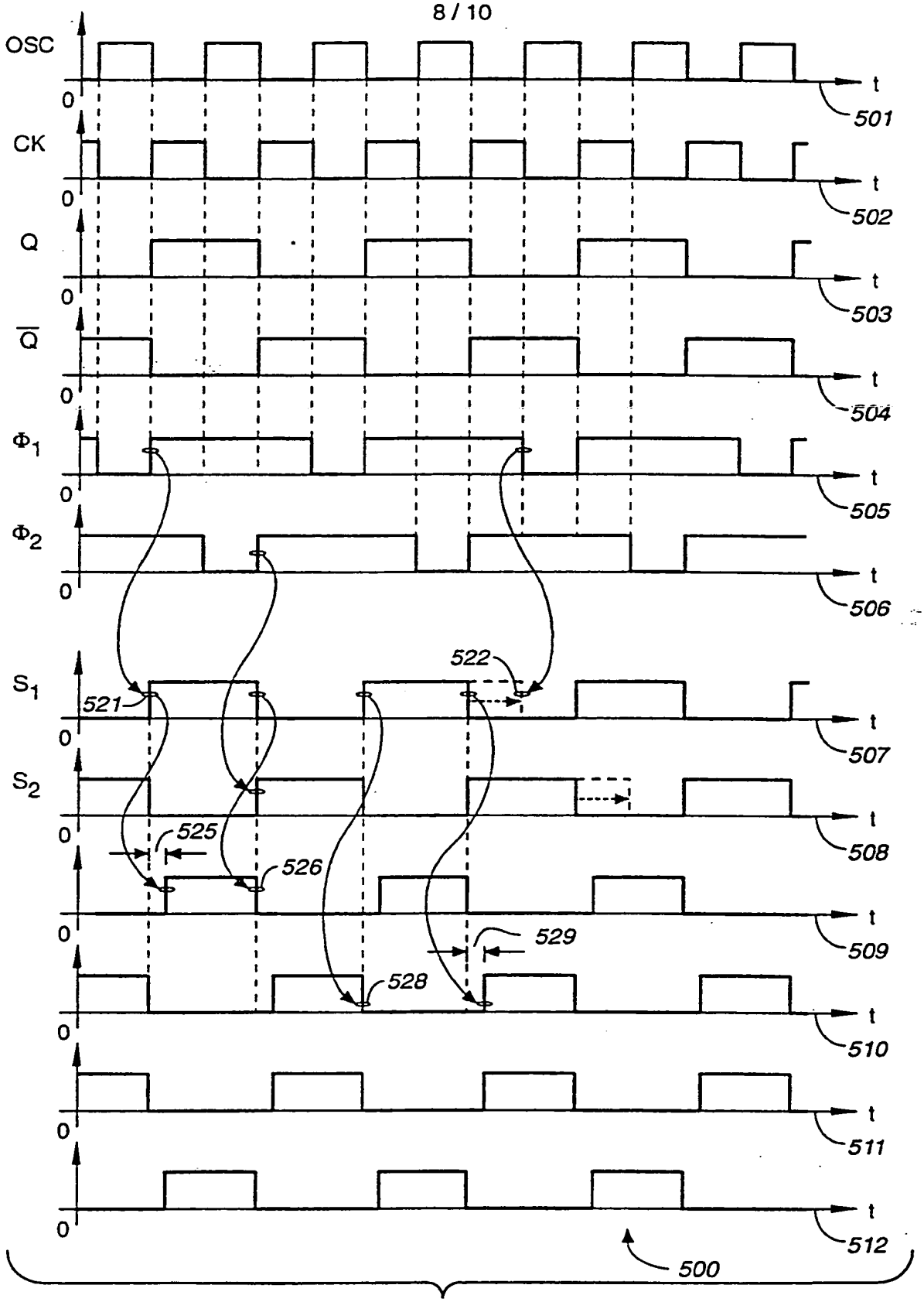
FIRST CONTROL MEANS
SECOND CONTROL MEANS
470
495
S_1
S_2
411
412
459
458
456
469
468
466
450
460
OUT
COMP
V_{FB}
R/C
I_S
GND
455
457
465
467
V_{CC}
410
Φ_1
Φ_2
421
435
436
438
437
430
433
431
432
434
Q
Q/
CK
D
DUAL CLOCK GENERATOR
452
453
451
446
445
444
449
448
447
420
OSC
1M
1MHz
428
429
425
426
427
424
441
440
442
418
417
416
415
V_{CC} (10v)
PWM MEANS
400
406
407
408
405

FIG._7


OSC
CK
Q
$\overline{Q}$
Φ_1
Φ_2
S_1
S_2
0
t
501
502
503
504
505
506
507
508
509
510
511
512
521
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525
526
528
529
500

FIG._8

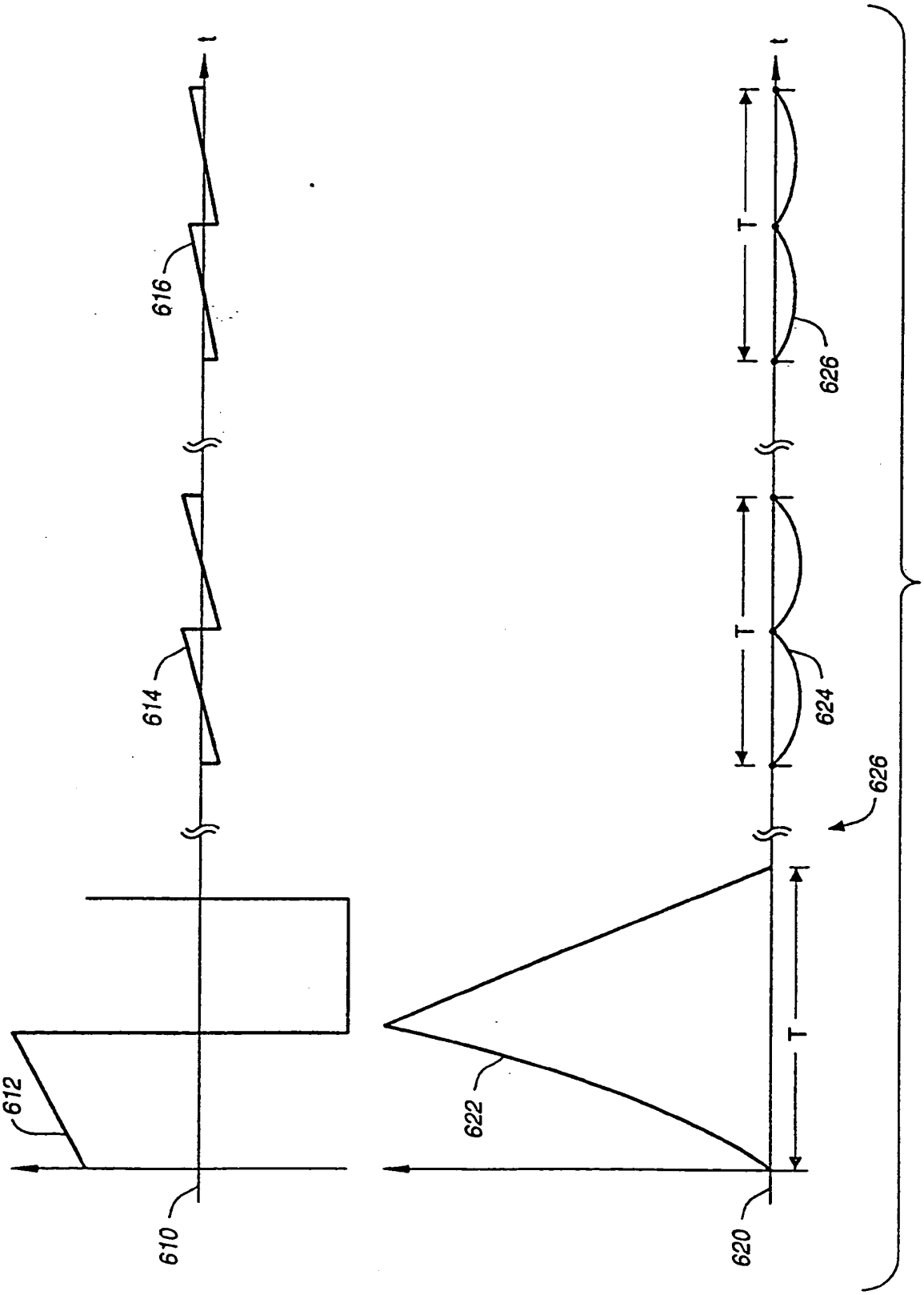


FIG._9

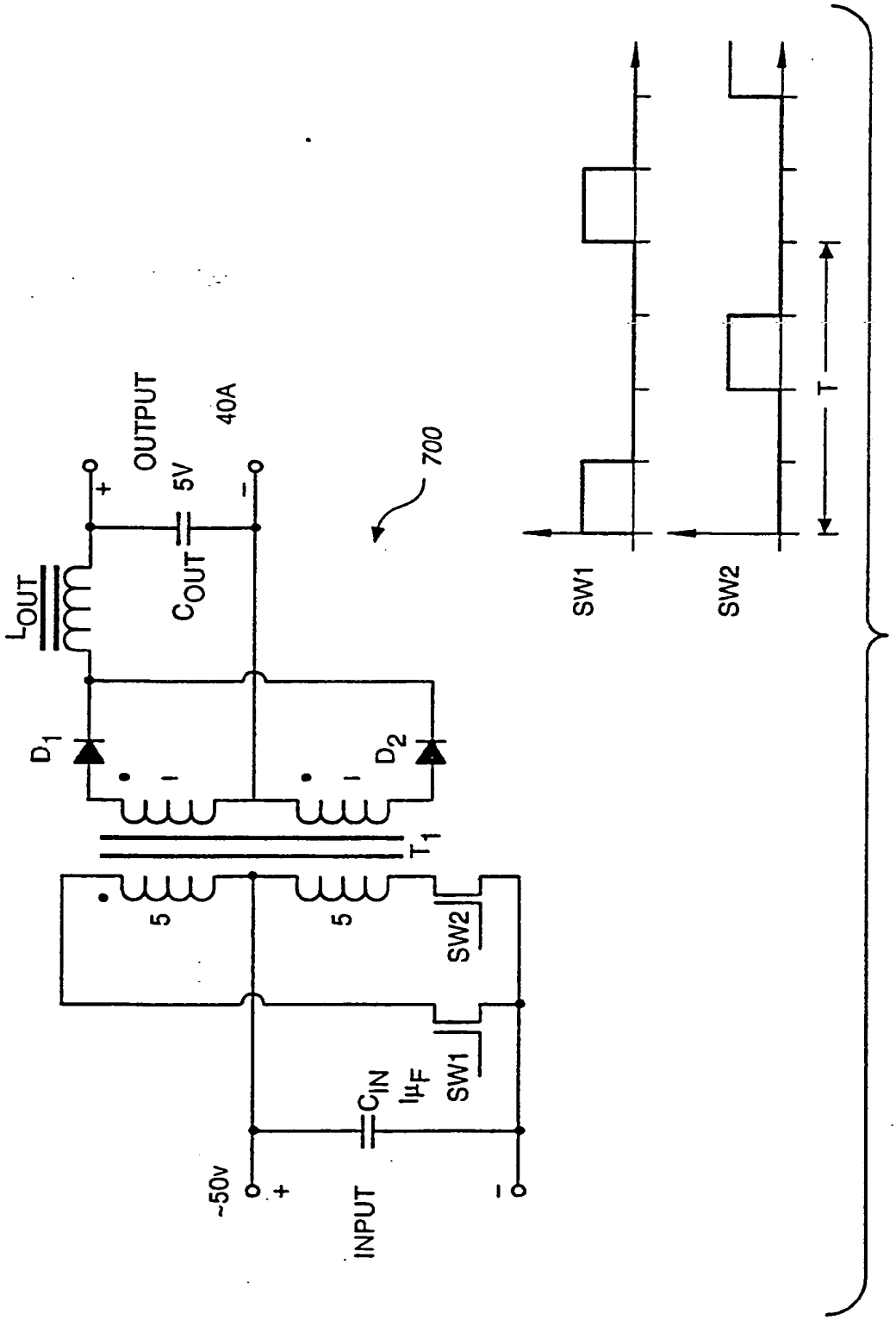


FIG._10
(PRIOR ART)

INTERNATIONAL SEARCH REPORT

International Application No PCT/GB 93/00877

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[5]: H 02 M 3/335, G 05 F 1/46

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[5]	H 02 M, G 05 F

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X	US, A, 5 088 017 (YAGINUMA et al.) February 11, 1992 (11.02.92), column 2, line 65 - column 3; line 40; column 4, lines 20-36; fig. 2; claims 1-5,11,12, 14,15.	1,2
A		6-11, 15,16
A	EP, A1, 0 483 897 (TELEFONAKTIEBOLAGET L M ERICSSON) May 6, 1992 (06.05.92), column 3, line 44 - column 5, line 3; fig. 1; claims 1,2,12.	1,2,7, 9,10
A	EP, A1, 0 162 374 (SIEMENS AG.) November 27, 1985 (27.11.85), page 6, line 12 - page 7,	1,2,6, 9,10

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
13 August 1993	01.09.93
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	MEHLMAUER e.h.

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, ** with indication, where appropriate, of the relevant passages	Relevant to Claim No.
	line 13; fig. 1; claims 1-5.	
A	US, A, 4 386 311 (BAFARO) May 31, 1983 (31.05.83), column 2, lines 48-52; claim 1.	1,10
A	DE, A1, 3 740 612 (PHILIPS) June 15, 1989 (15.06.89), abstract; claim 1.	1,10

ANHANG

zum internationalen Recherchenbericht über die internationale Patentanmeldung Nr.

ANNEX

to the International Search Report to the International Patent Application No.

ANNEXE

au rapport de recherche international relatif à la demande de brevet international n°

PCT/GB 93/00877 SAE 73940

In diesem Anhang sind die Mitglieder der Patentfamilien der im obengenannten internationalen Recherchenbericht angeführten Patentdokumente angegeben. Diese Angaben dienen nur zur Unterrichtung und erfolgen ohne Gewähr.

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The Office is in no way liable for these particulars which are given merely for the purpose of information.

La présente annexe indique les membres de la famille de brevets relatifs aux documents de brevets cités dans le rapport de recherche international visée ci-dessus. Les renseignements fournis sont donnés à titre indicatif et n'engagent pas la responsibilité de l'Office.

Im Recherchenbericht angeführtes Patentdokument Patent document cited in search report Document de brevet cité dans le rapport de recherche	Datum der Veröffentlichung Publication date Date de publication	Mitglied(er) der Patentfamilie Patent family member(s) Membre(s) de la famille de brevets	Datum der Veröffentlichung Publication date Date de publication
US A 5088017		EP A2 348873	03-01-90
		EP A3 348873	17-07-91
		DE CO 68906968	15-07-93
		EP B1 348873	09-06-93
		US A 4954600	04-09-90
		JP A2 2084432	26-03-90
EP A1 483897	06-05-92	CA AA 2053737	25-04-92
		SE AO 9003399	24-10-90
		SE A 9003399	25-04-92
		SE B 467384	06-07-92
		SE C 467384	29-10-92
		US A 5229928	20-07-93
EP A1 162374	27-11-85	AT E 46233	15-09-89
		DE CO 3572900	12-10-89
		EP B1 162374	06-09-89
		JP A2 61018367	27-01-86
		NO A 851857	11-11-85
		NO B 165089	10-09-90
		NO C 165089	19-12-90
		US A 4669039	26-05-87
US A 4386311	31-05-83	keine - none - rien	
DE A1 3740612	15-06-89	keine - none - rien	

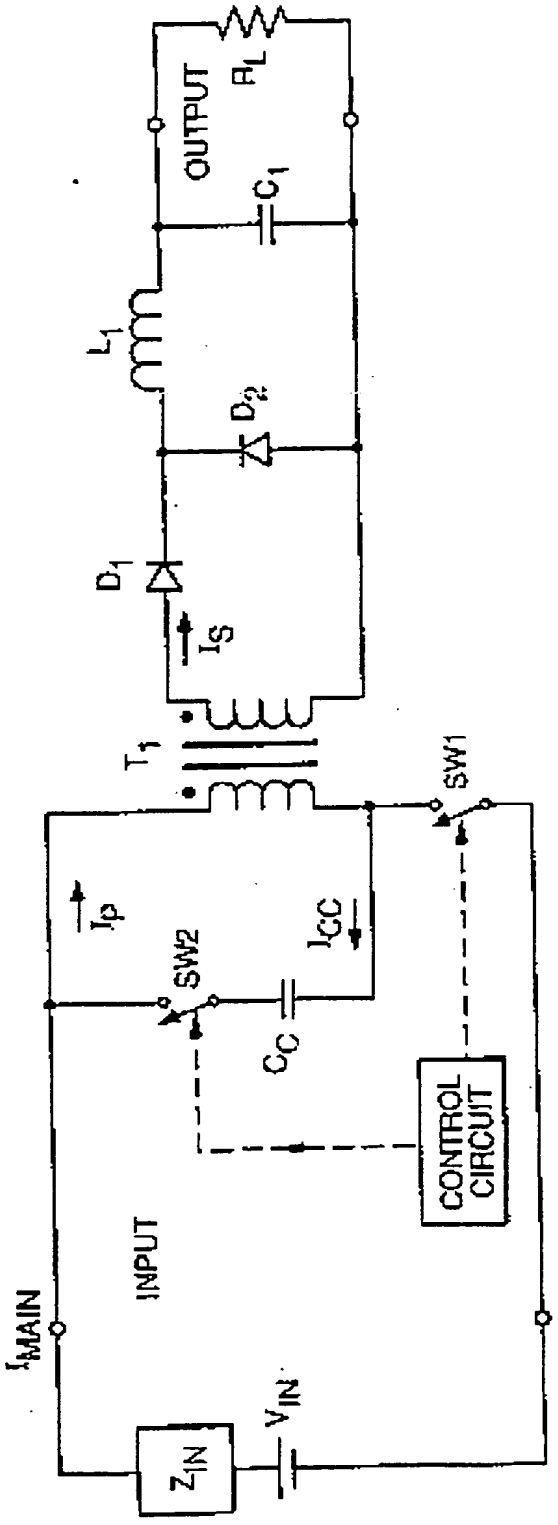


FIG._1
(PRIOR ART)

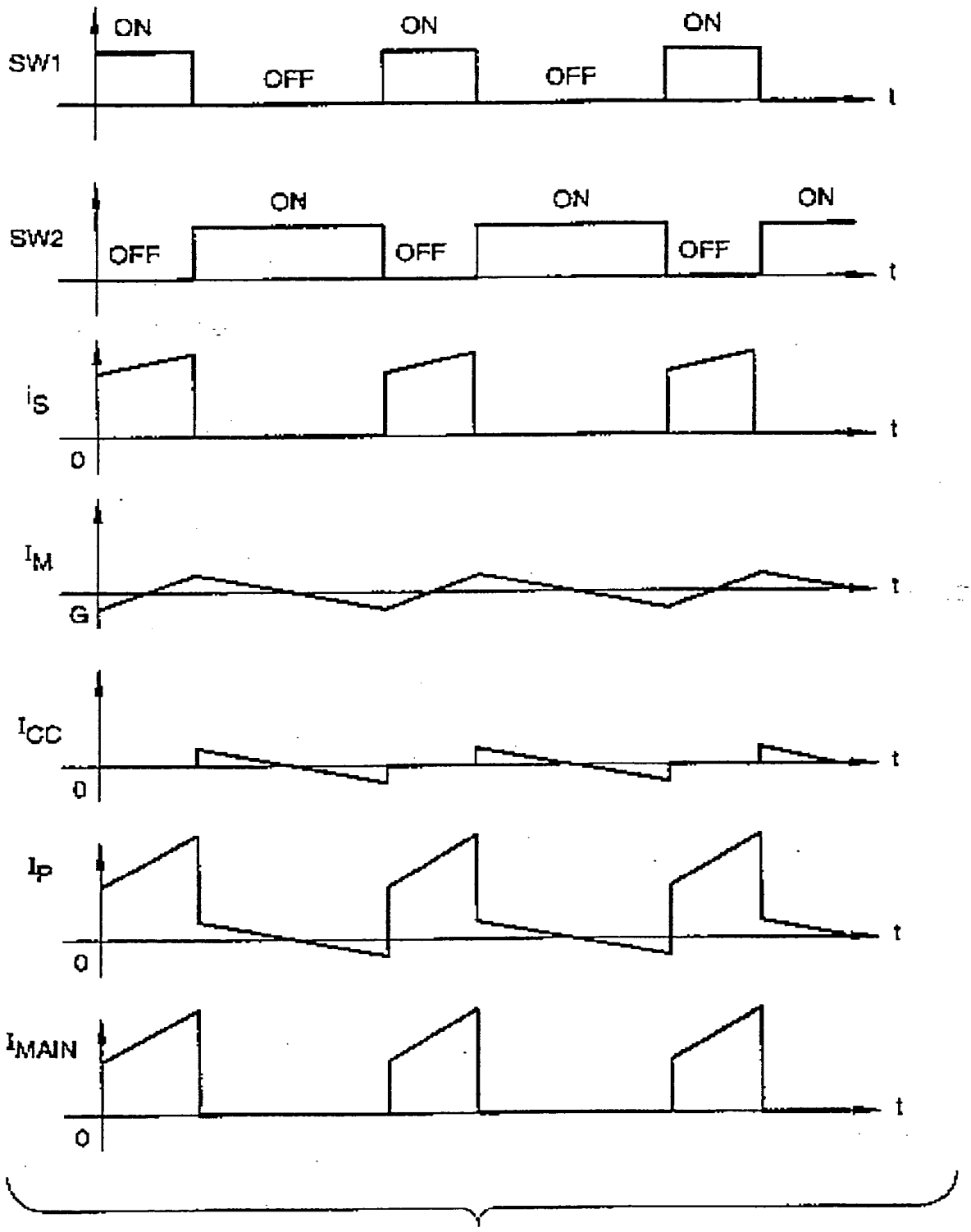
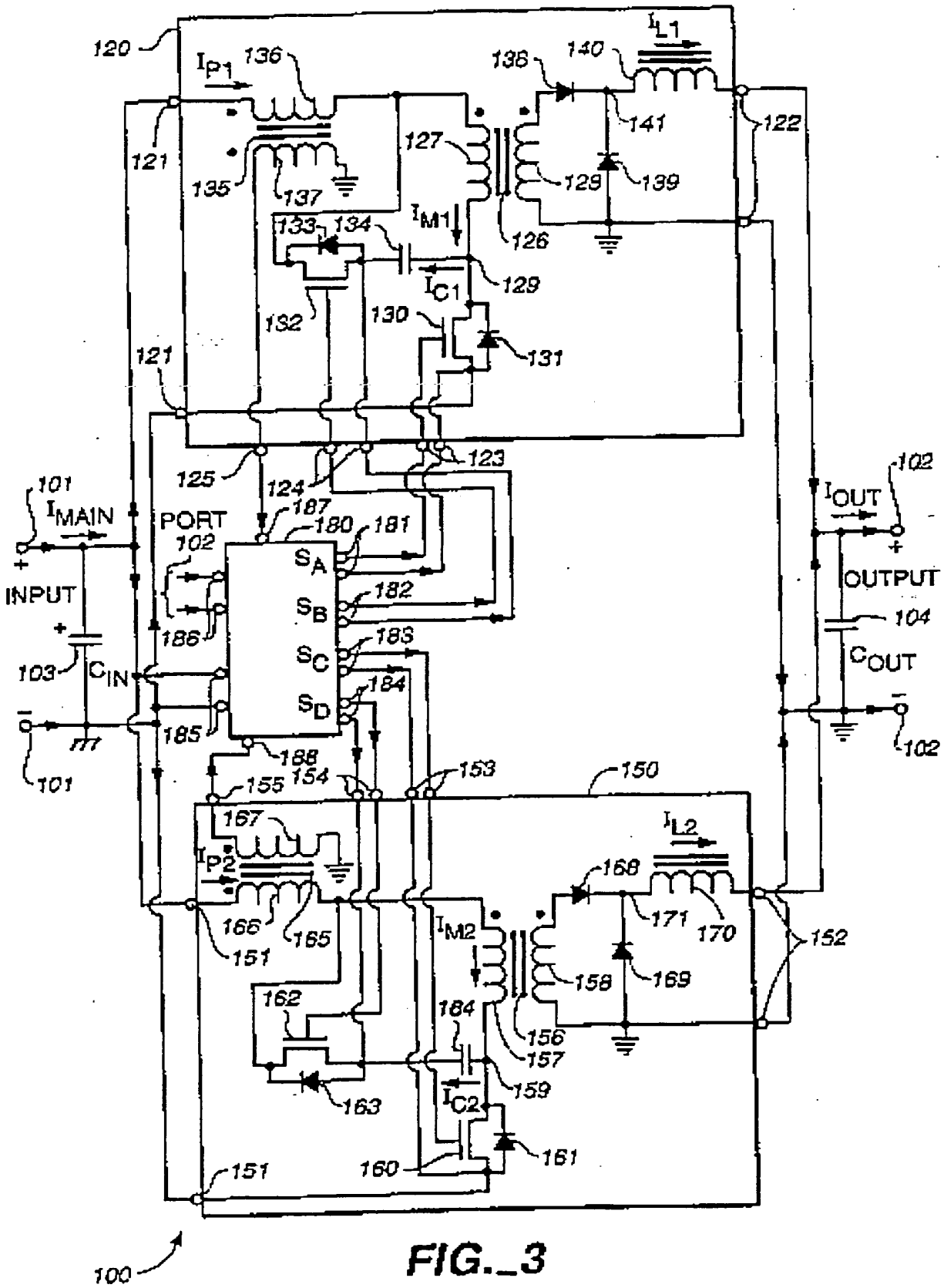


FIG._2
(PRIOR ART)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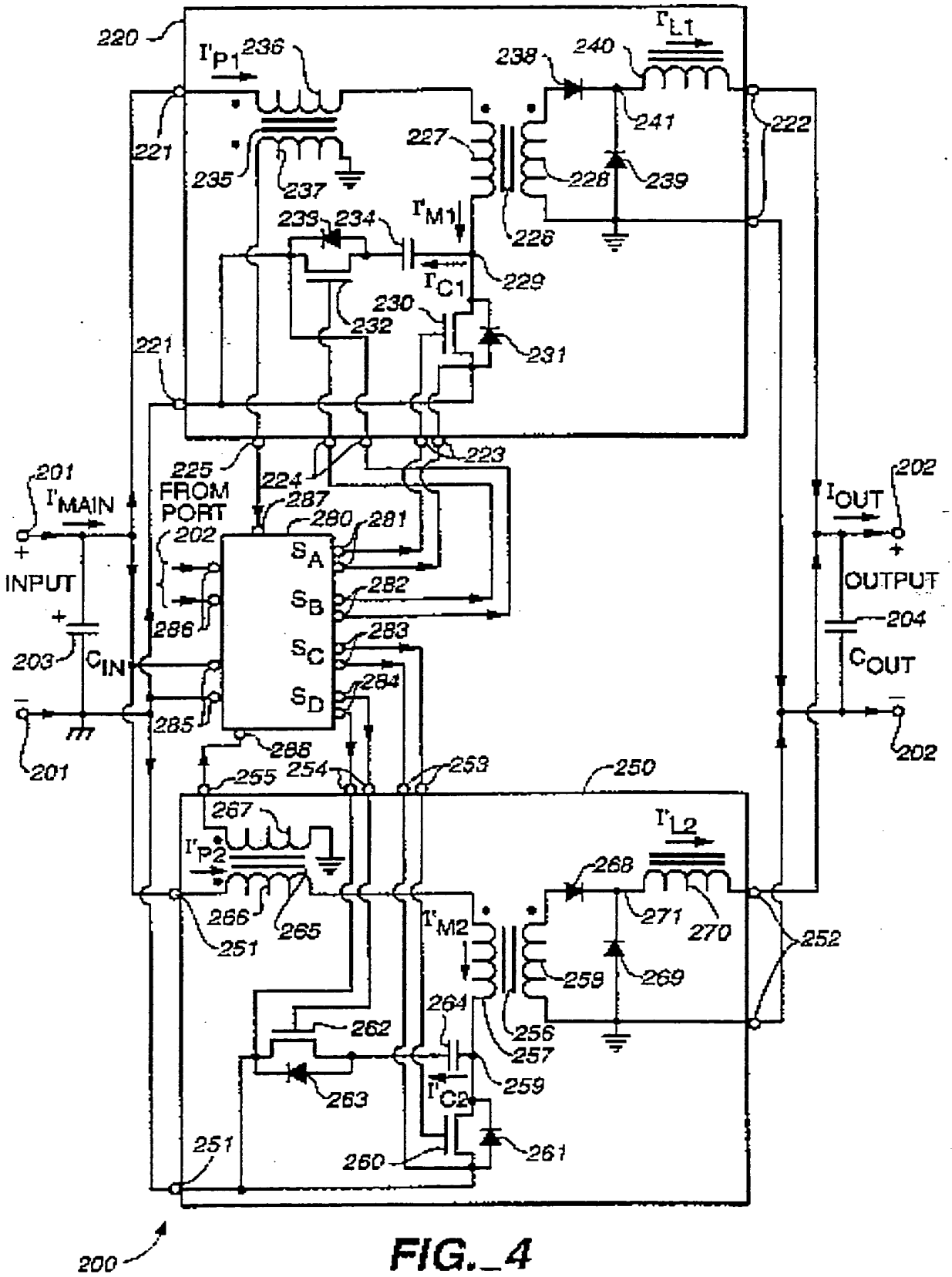
129
I_{C1}
132
130
131
121
123
125
124
187
180
181
101
I_{MAIN}
PORT
102
S_A
S_B
S_C
S_D
182
183
184
186
185
188
INPUT
103
C_{IN}
101
155
154
153
150
167
I_{P2}
166
165
151
I_{L2}
168
171
170
152
I_{M2}
158
169
162
164
156
157
159
163
I_{C2}
161
160
151
I_{OUT}
102
OUTPUT
104
C_{OUT}
102
100

FIG._3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I'_{P1}
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I'_{L1}
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240
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221
235
237
227
228
239
226
233
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I'_{M1}
229
I'_{C1}
230
232
231
221
223
225
FROM PORT
224
287
280
281
201
I'_{MAIN}
INPUT
202
S_A
S_B
S_C
S_D
282
283
284
286
203
C_{IN}
285
288
201
255
254
253
250
I_{OUT}
202
OUTPUT
204
C_{OUT}
202
267
I'_{P2}
I'_{L2}
268
266
265
271
270
251
I'_{M2}
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269
252
264
262
256
257
259
263
I'_{C2}
251
260
261
200

FIG._4

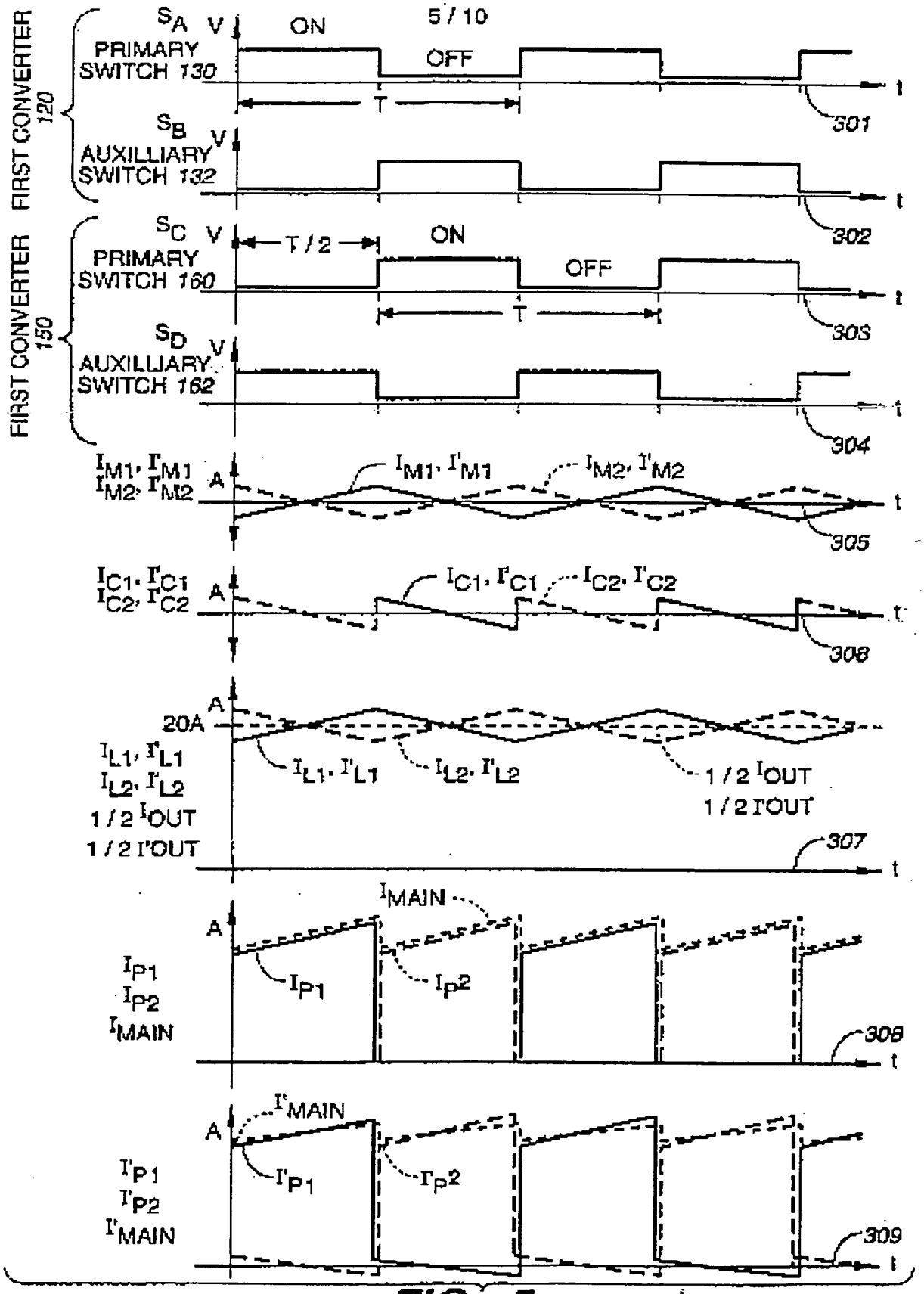

FIRST CONVERTER 120
FIRST CONVERTER 150
S_A V
PRIMARY SWITCH 130
ON
OFF
T
t
301
S_B V
AUXILLIARY SWITCH 132
302
S_C V
T / 2
PRIMARY SWITCH 160
303
S_D V
AUXILLIARY SWITCH 162
304
I_{M1}, I'_{M1} I_{M2}, I'_{M2}
A
305
I_{C1}, I'_{C1} I_{C2}, I'_{C2}
306
20A
I_{L1}, I'_{L1}
I_{L2}, I'_{L2}
1 / 2 I_{OUT}
1 / 2 I'_{OUT}
307
I_{MAIN}
I_{P1}
I_{P2}
308
I'_{MAIN}
I'_{P1}
I'_{P2}
309
300

FIG._5

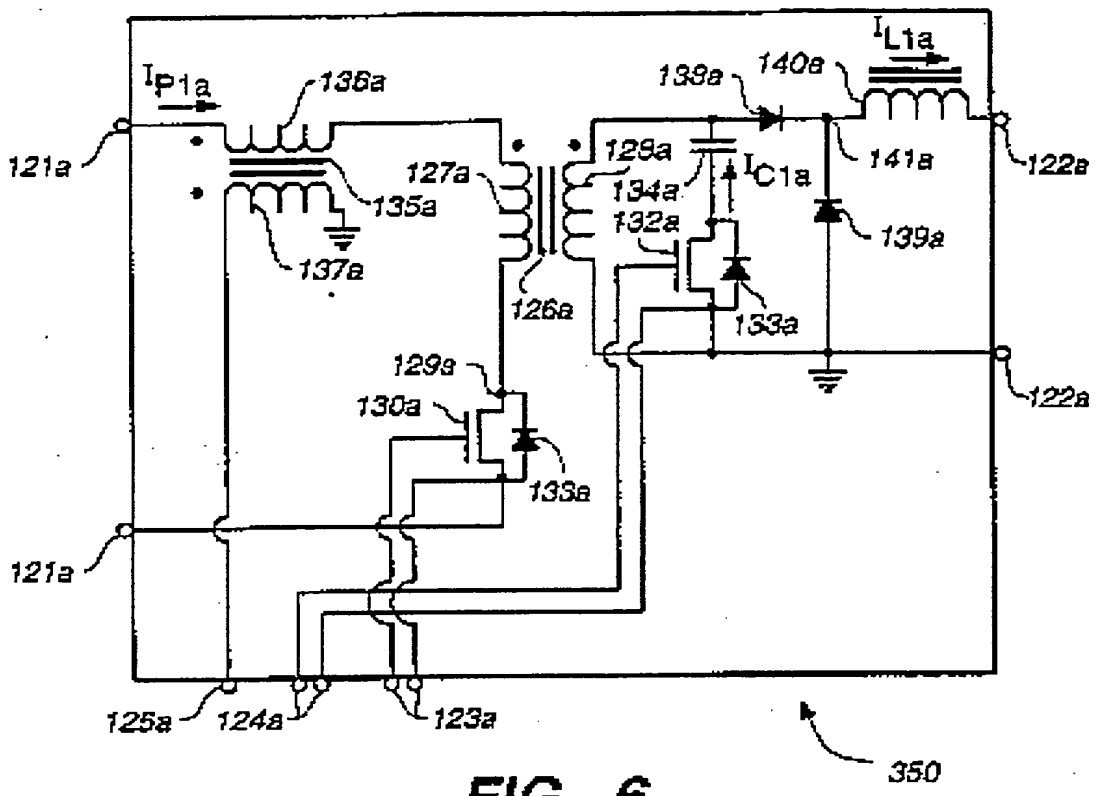

I_{P1a}
136a
121a
135a
127a
137a
126a
129a
134a
132a
I_{C1a}
133a
139a
140a
I_{L1a}
141a
122a
129a
130a
133a
121a
125a
124a
123a
350

FIG._6

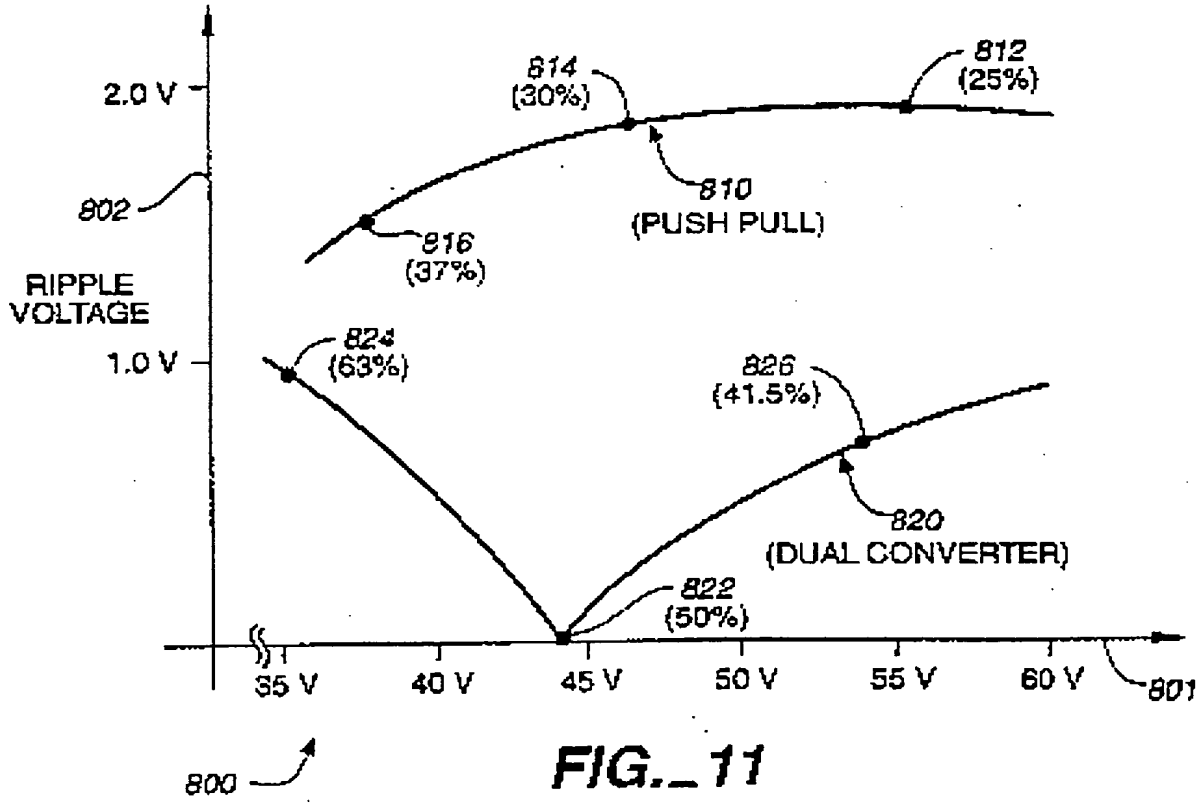
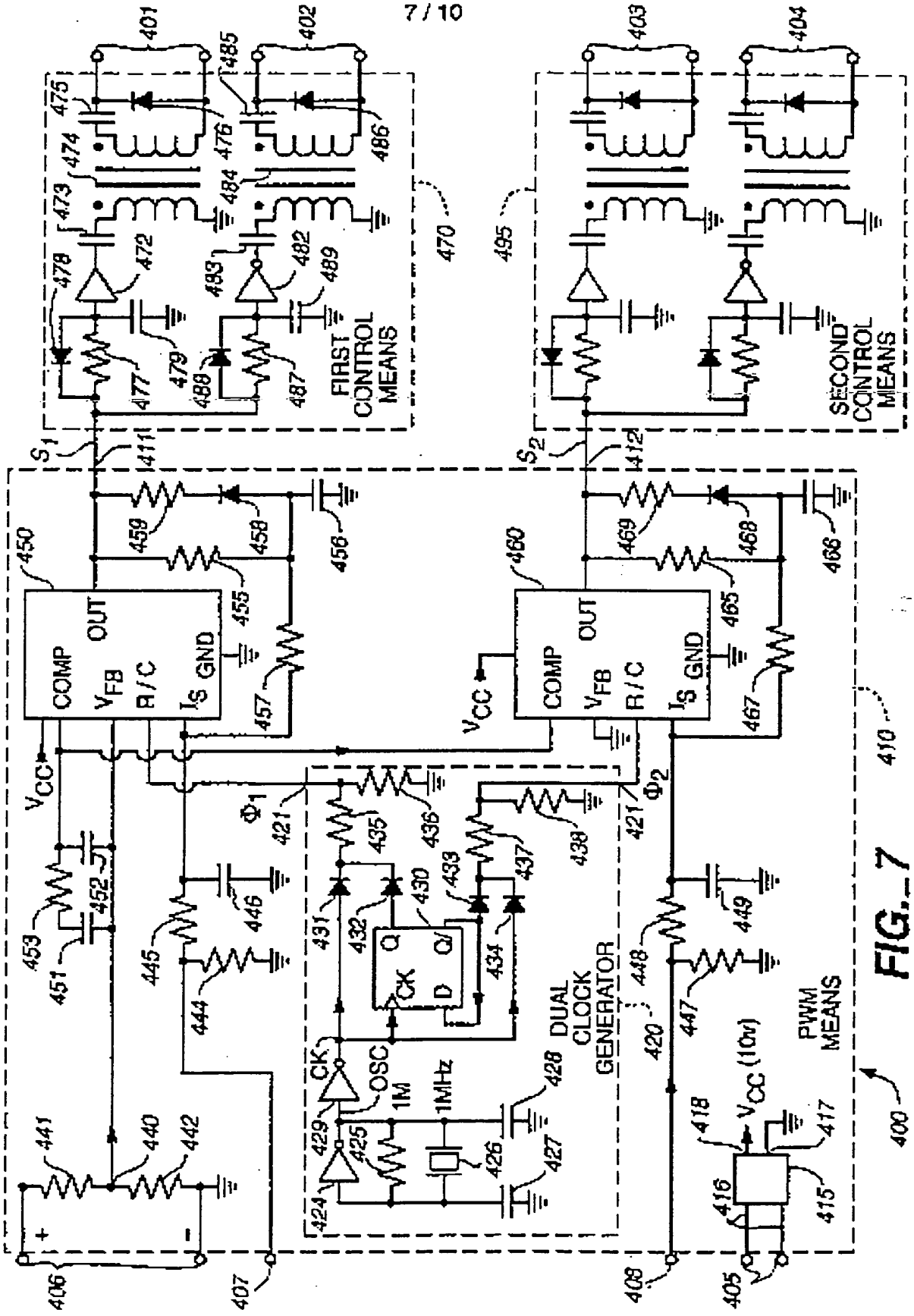

2.0 V
802
RIPPLE VOLTAGE
1.0 V
814 (30%)
812 (25%)
810 (PUSH PULL)
816 (37%)
824 (63%)
826 (41.5%)
820 (DUAL CONVERTER)
822 (50%)
35 V
40 V
45 V
50 V
55 V
60 V
801
800

FIG._11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477
FIRST CONTROL MEANS
470
495
SECOND CONTROL MEANS
S1
411
S2
412
450
460
459
458
456
469
468
466
455
465
457
467
OUT
COMP
VFB
R/C
IS
GND
VCC
410
Φ1
Φ2
421
435
436
438
437
452
446
449
453
451
445
444
448
447
431
432
430
433
434
Q
Q/
CK
D
DUAL CLOCK GENERATOR
OSC
1M
1MHz
428
429
425
426
427
424
420
PWM MEANS
VCC (10v)
418
417
416
415
441
440
442
400
406
407
408
405

FIG._7

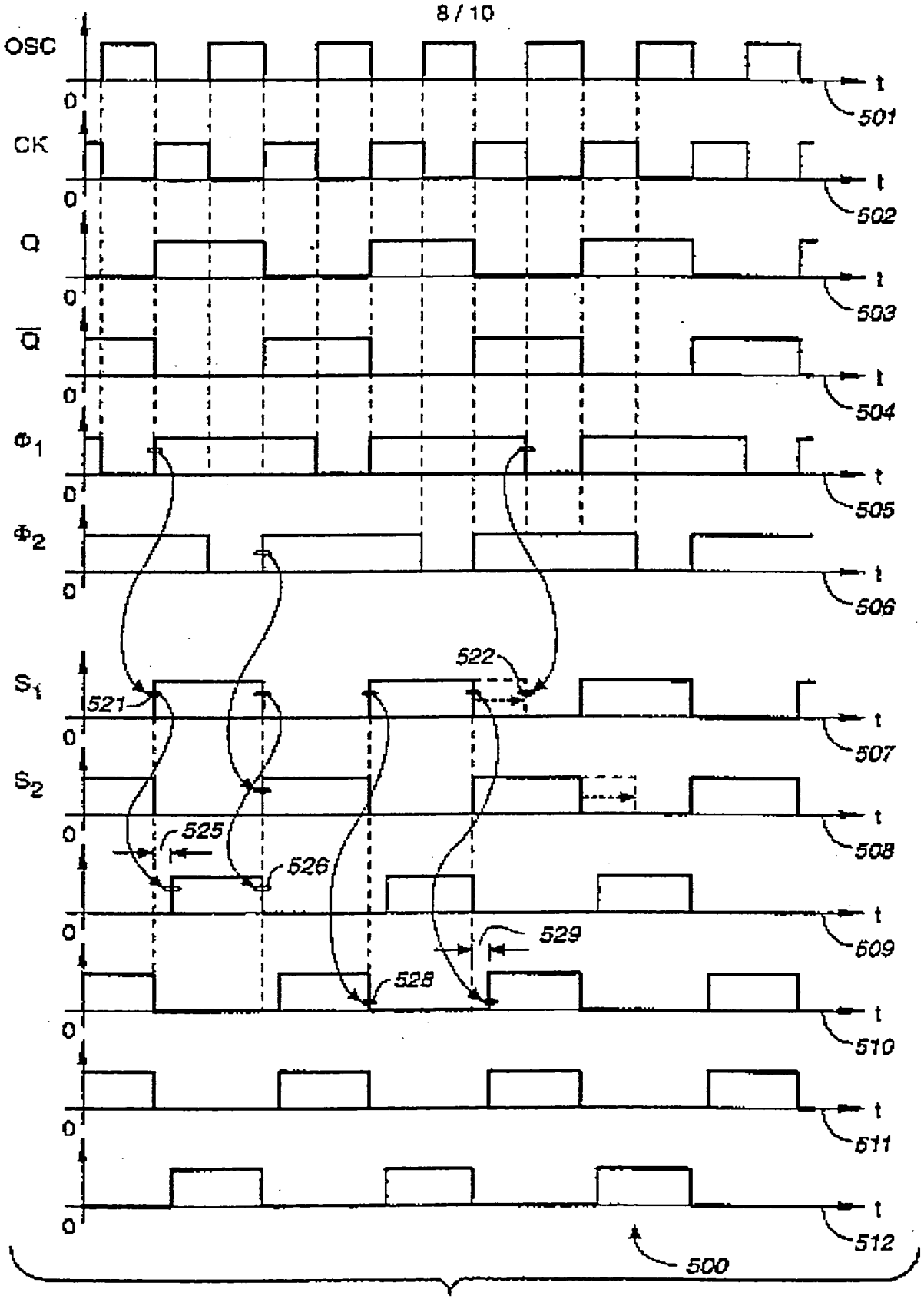
OSC
CK
Q
$\overline{Q}$
Φ_1
Φ_2
S_1
S_2
0
t
501
502
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FIG._8

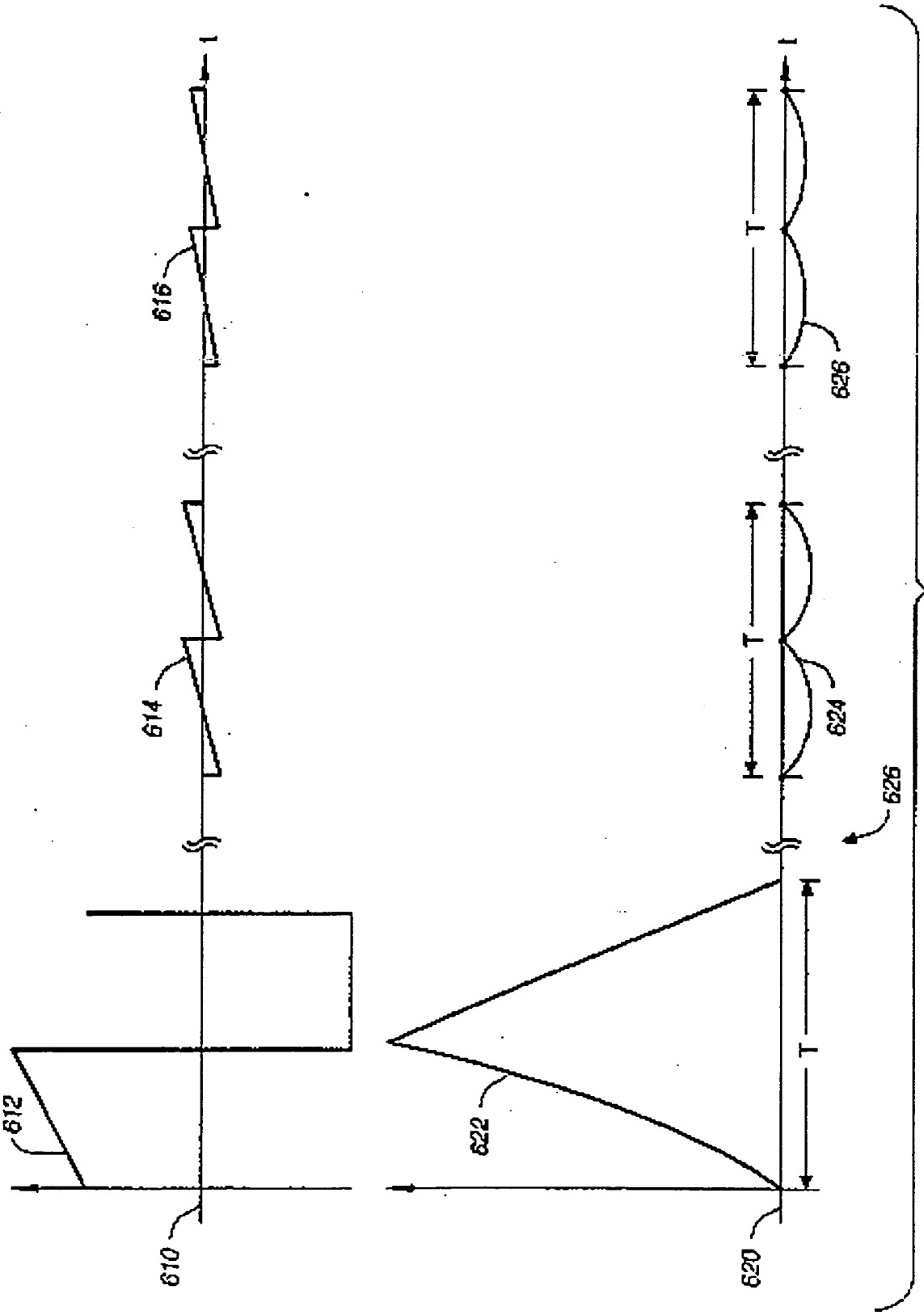

FIG._9

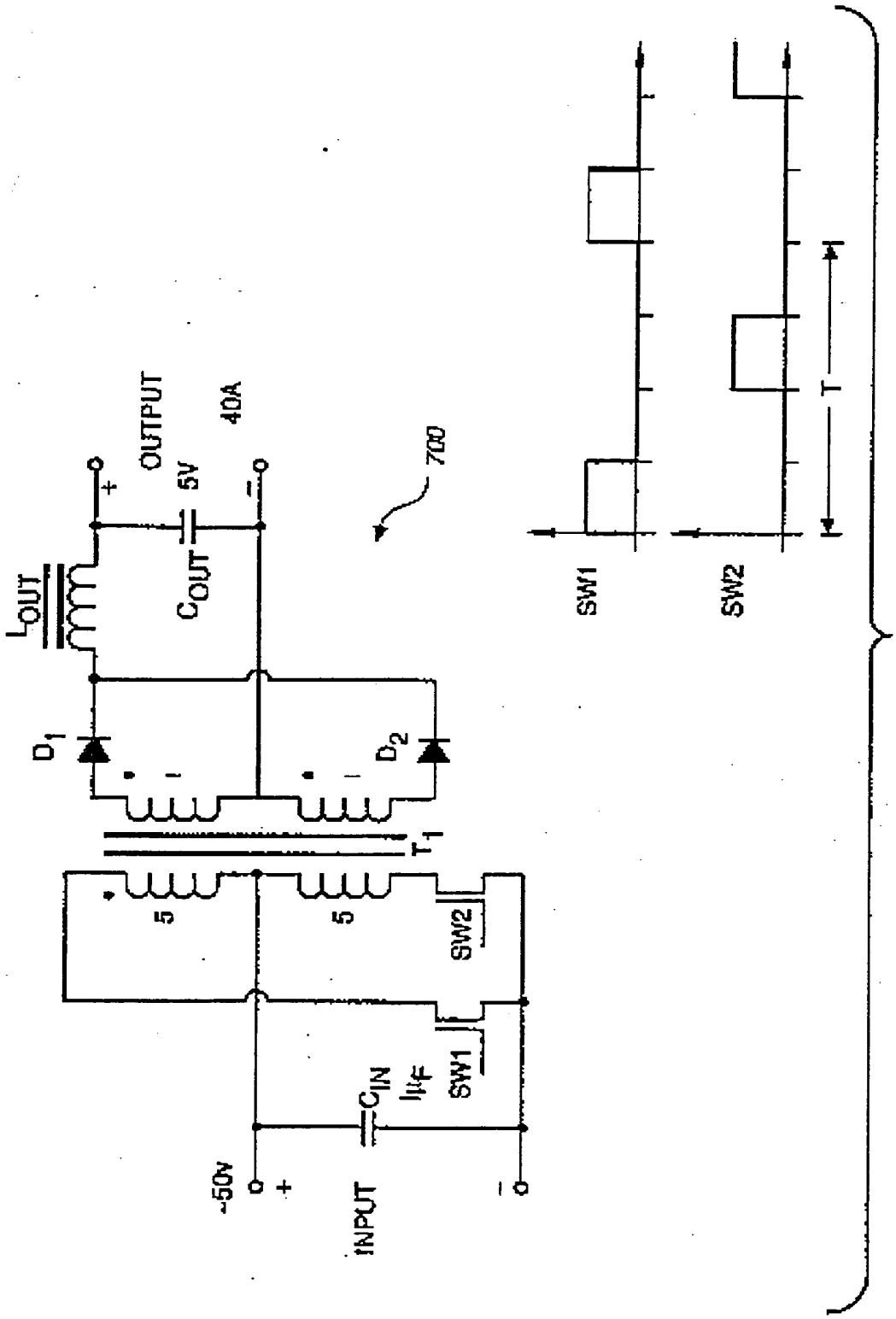

FIG._10
(PRIOR ART)